ADH8066 Quad band GSM/GPRS Module

Hardware Application Note
<V1.3>

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Change History

Version	Effective Date	Description of Changes
V1.0	2009/8/7	Released
V1.1	2009/12/11	Update standby power consumption
V1.2	2010/6/25	Add ONKEY & DSR circuit recommendation
V1.3	2010/7/30	Modify PWR ON/OFF sequence

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1. ADH8066 Key Features

Table 1: ADH8066 key feature list

Product features	Descriptions
Frequency	GSM 850/ GSM900/GSM1800 /GSM1900 Quad Band
Maximum RF Power	GSM850/EGSM900 Class4 (2W)
	GSM1800 GSM 1900 Class1 (1W)
Receiving Sensitivity	<-106dBm
Working Temperature	-30°C～+70°C (with SIM holder) -40°C～+85°C (without SIM holder)
Power Voltage	3.4V～4.5V (4.0V is recommended)
Average STB current	<2mA@paging mode 6 (Standby mode)
Leaking current	<0.1mA
Protocol	Support GSM/GPRS Phase2/2+
AT COMMAND	GSM Standard AT COMMAND
	V.25 AT COMMAND
	AMOD defined AT COMMAND
50PIN B2B Connector	UART Interface (Maximum I/O speed: 115200bit/s)
SIM interface	Standard SIM interface (3V/1.8V)
Audio interface	2 Analogue audio Input/Output interfaces
Power interface	Power interface
GSC RF Connector	50Ω RF Antenna Connector
Voice Communication	Support FR, EFR, HR and AMR voice codec
	Support hands free operation and echo exhibition.
SMS	Support MO and MT
	Support Point-to-Point Short Message Cell Broadcast
	Support TEXT and PDU mode
GPRS Data transmission	GPRS CLASS 10
	Coding scheme CS 1, CS 2, CS 3, CS 4
	Maximum transmission speed: 85.6Kbit/s [1]
	Support PBCCH
	Built-in TCP/IP protocol. Support multi-slot, ACK response, support large memory buffer.
CSD Service	Support CSD data transmission up to 9600bit/s
	Fax support: Group3, Class1.0
	Support USSD
Supplemental service	Caller ID, Call transfer.
Group Service	Support group call, broadcast, Group call service & broadcast service
STK[2]	Support STK through enhanced AMOD AT COMMAND

[1] Depending on network condition
[2] Upon customer request

2. System Architecture

Figure 1 describes ADH8066 function diagram and main system interface.

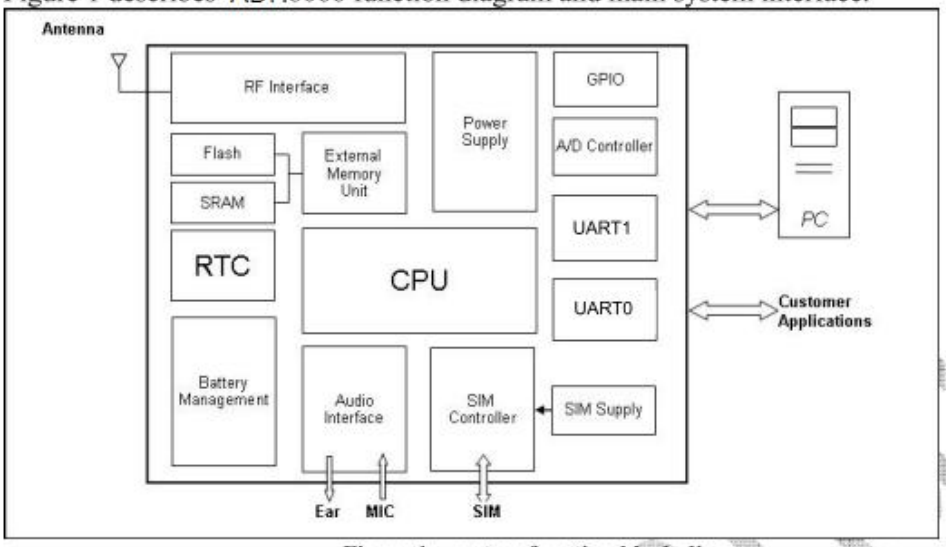


Figure 1: . system function block diagram

3. Power Supply Recommendations

3.1 Ground Connections Recommendations

The PCB right under ADH8066 should be left as a ground plane which SHOULD NOT have any components or layout circuit in case of RF interference.

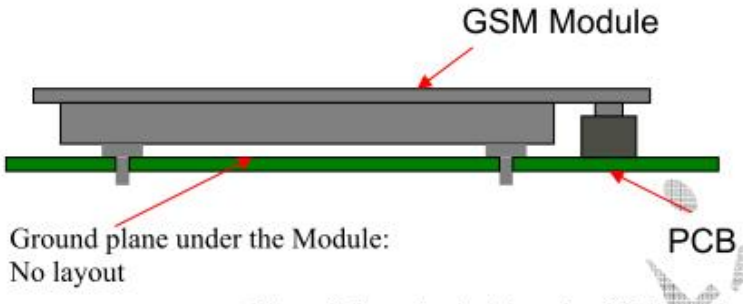


Figure 2: Layout principle under GSM module

3.2 Power Supply Generalities

Power supply design is critical to GSM module applications. The design guides should be strictly followed to ensure the performance of the module. The VBAT voltage limits must be at any time: 3.4V <VBAT< 4.5V. The worst condition is during the burst period transmission, when current consumption is at its highest. During this period, the VBAT voltage is reduced to the lowest level:

- The output voltage of the power supply drops.
- Voltage drop is present between the power supply output and the GSM module supply pins (VBAT).

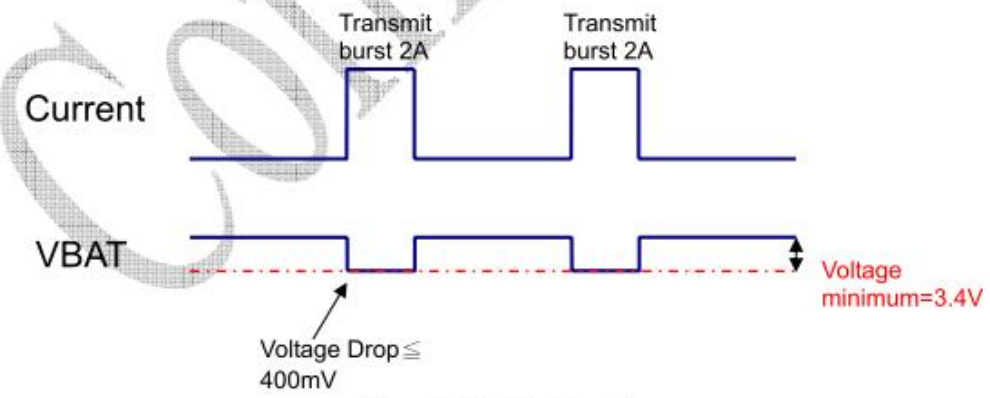


Figure 3: VBAT voltage drop

3.3 Voltage Versus Distance

Depending on the distance between the power supply and the GSM module, behavior is described as figure 4:

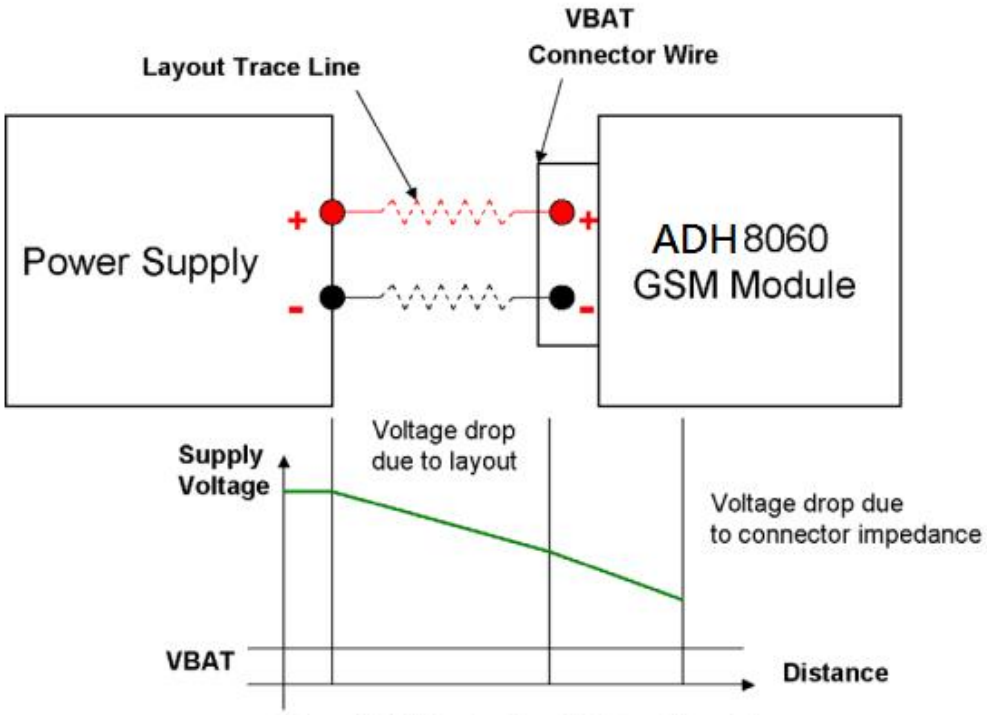


Figure 4: Voltage drop versus distance

3.4 Design Recommendation

Additional notes to the design of power supply circuit:

- Quality attention must be paid to the power supply circuit for their resistance value and burst current.
- The circuit line between power supply input to VBAT should try to avoid interference of other source of signals.
- Decoupling capacitors.

3.4.1 Power Supply Selection

Power supply selection must fulfill following conditions:

- By using large capacity and low ESR capacitors, the system can avoid influence of over burst current.
- The power sources must have good ripple rejection. In another word, the ripple value of current input to VBAT should be as low as possible.
- Low output resistance.

3.4.2 Power Supply Circuit Recommendation

Interferences of other signal sources to the power supply must be avoided.

VBAT connection pins: Pins 26, 27, 28, 29, 30

- Track line width between the power supply and GSM VBAT input should be 3mm.
- The power circuit lines should be separated from other signal lines (e.g.

Audio/SIM/UART… etc) by ground

- Makes sure to avoid having any signal lines going under the power lines.
- D01 of the input side is used to avoid over voltage of burst current to damage internal circuit. It can also avoid wrong connection of positive and negative poles.
- R02/R03 of the output side is to adjust output voltage
- Value of C06/C07 is 330uF and needs to be Low ESR capacitors.

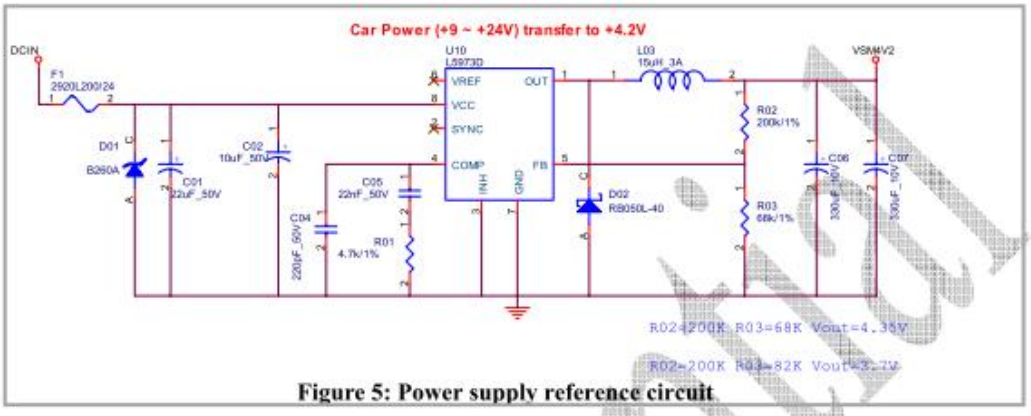


Figure 5: Power supply reference circuit

3.4.3 Power ON & reset circuit recommendation

User can use ON_KEY (PIN 41) for system reset. Pull low for 300ms to active to re-power on the system.

Power on reset recommendation circuit works as follow principles:

1. Before power on, VDD_TOP=Low, ON_KEY=Low
2. When the power ON, VDD_TOP=High, ON_KEY=High
3. If the system crashes then the VDD_TOP is pulled low and ON_KEY is pulled high automatically to reset the system by software.
4. VDD_TOP is always high if system function normally. User can use GPIO to detect VDD_TOP status. (VDD_TOP=PIN31, output voltage 1.8V)

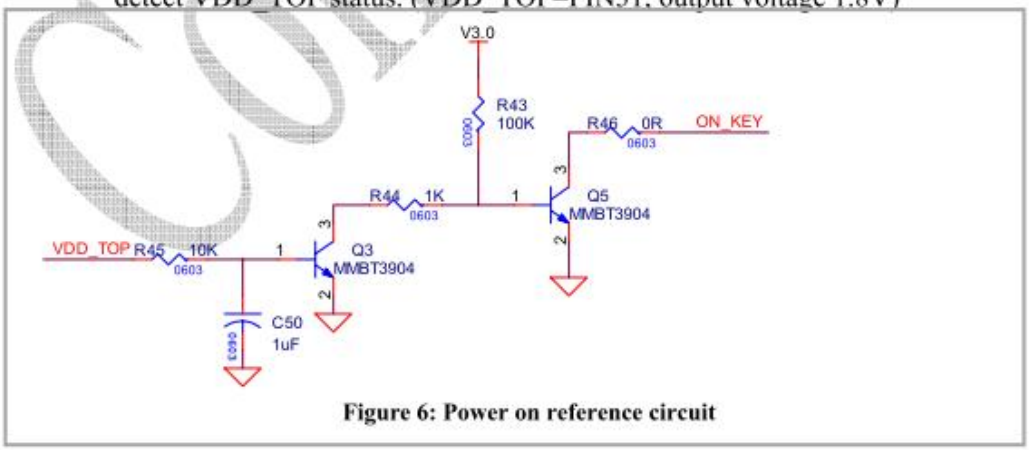


Figure 6: Power on reference circuit

3.4.4 Decoupling capacitors

The value of decoupling capacitors is 33pF/100uF, and recommended location is close

to the VBAT supply pins. The purpose of these decoupling capacitors is to avoid EMI interferences.

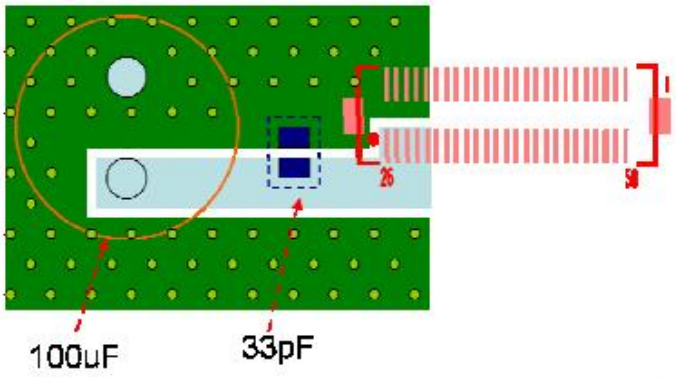


Figure 7: Value of decoupling capacitors

4. Interfaces

4.1UART Interface

4.1.1 UART interface characteristic and pin out description

ADH8066 has two UARTs, both are available on the bottom connector.
UART0 is used to communicate with host systems, and to download the memory FLASH. The interface configuration is described as follow tables:

Table 2: UART Data configuration

Description	Configurations
Baud rate	115,200
Data bits	8 bits
Stop bit	1
Parity check	Non
HW flow control	Non

Table 3: UART0 pin out description

UART0	Connector Pin	Description
RXD0	17	Receive Data
TXD0	15	Transmit Data
DCD0	39	Data Carrier Detected
DTR0	33	Data Terminal Ready
DSR0	35	Data Set Ready
RTS0	37	Request To Send
CTS0	34	Clear to Send
RI0	32	Ring Indication

Table 4: UART1 pin out connector

UART1	Connector Pin	Description
RXD1	16	Receive Data
TXD1	14	Transmit Data

Table 5: Electrical characteristics

ITEM	Description	UART0 interface (UART1 for system)	
		MIN	MAX
Vil	Low level voltage input		(0.3 x VDD_IO_HIGH) 0.87V
Vih	high level voltage input	(0.7 x VDD_IO_HIGH) 2.03V	
Vol	Low level voltage Output		0.4 V
Voh	High level voltage output	(VDD_IO_HIGH-0.4V) 2.5V	

Iil	Low level input current		1 µA
Iih	High level input current		1 µA
Iol	Low level output current		4 mA
Ioh	High level output current		-4 mA

The ESD/EMI IC has internal resistors in the range of 72 W to 88W.

4.1.2 UART0 interface reference circuit design

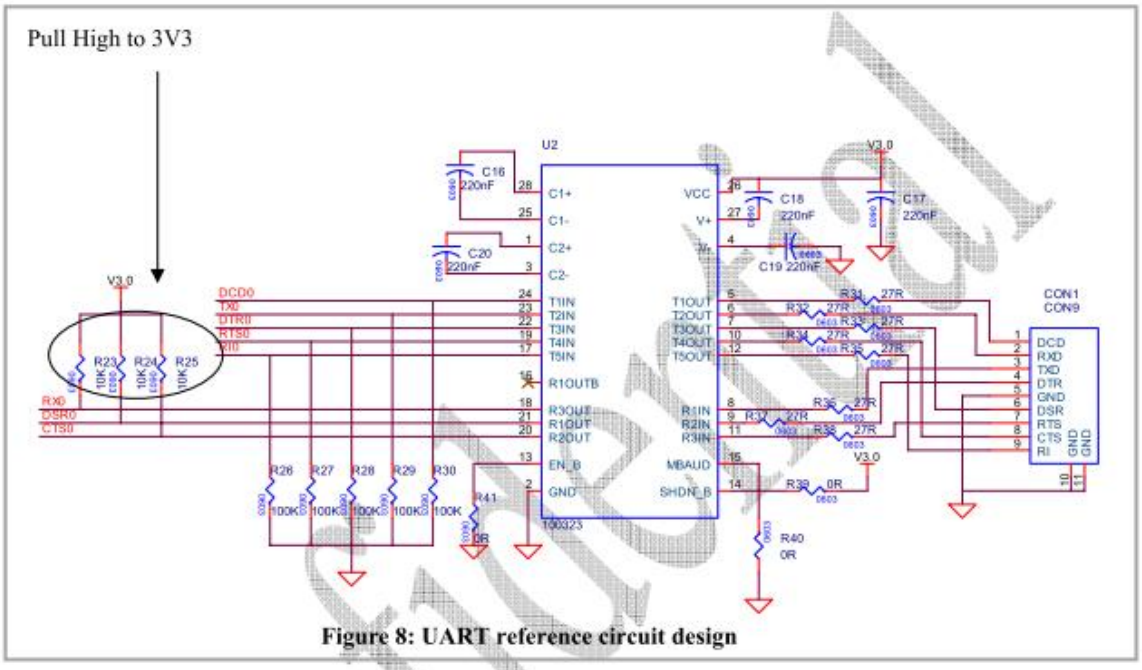


Figure 8: UART reference circuit design

4.2 Audio Interface

Two different microphone inputs and two speaker outputs are supported on ADH8066.

4.2.1 Audio track and PCB Layout Recommendation

To avoid TDMA noise, it is recommended to surround the audio tracks by ground:

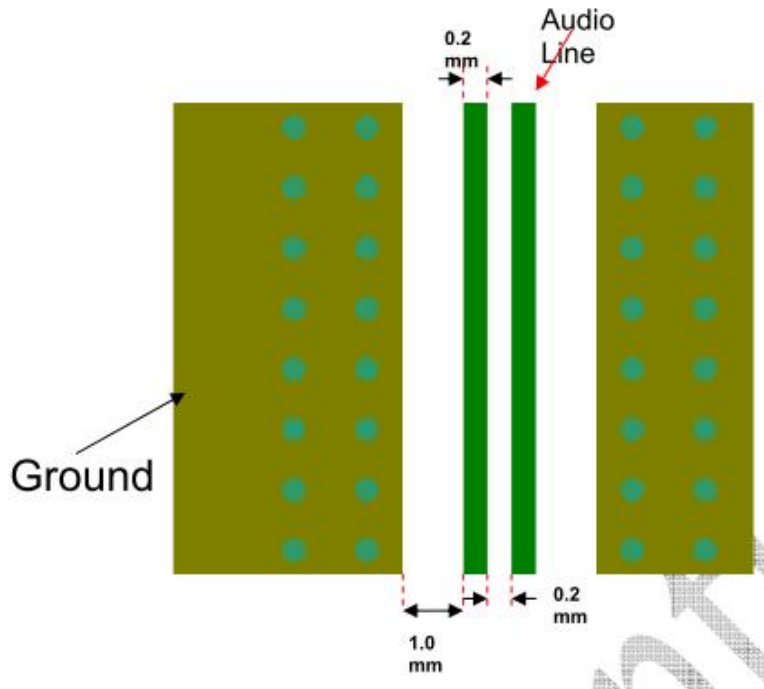


Figure 9: Audio track design

4.2.2 Microphone Inputs

The MIC1 and MIC2 inputs already include the biasing for an electric microphone, allowing easy connection to a headset. The circuit design is as below picture. Please note that Audio_GND (Pin42) needs to be connected to Audio Jack GND.

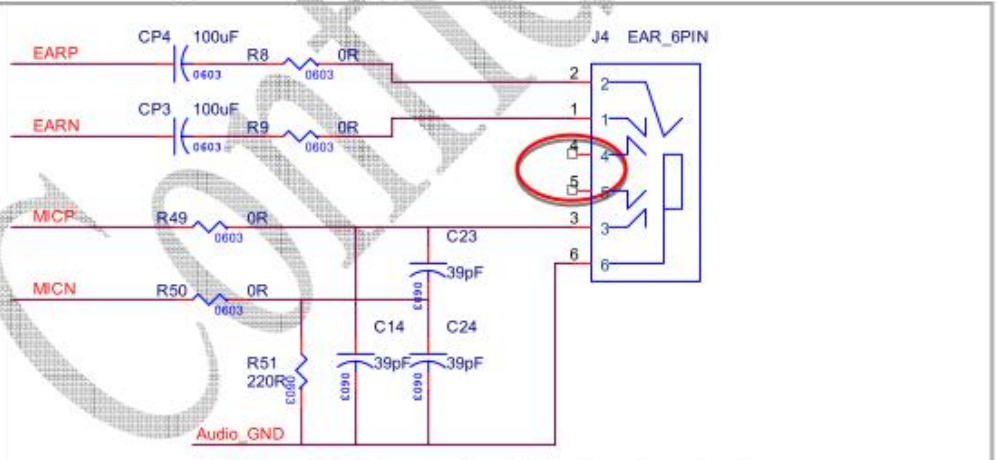


Figure 10: Reference circuit for microphone inputs

4.3 SIM Interface

ADH8066 supports 1.8V and 3.3V SIM cards. SIM_VCC can be connected to 1.8V or 3.3V power source.

4.3.1 SIM interface circuit design

ADH8066 has with SIM holder without SIM holder version. If you chose to use ADH8066 without SIM holder, please pay attention to place two capacitors in the circuit design described as follows:

1. 10μF: close to the GSM module connector;
2. 100nF: close to the SIM connector.

These two capacitors are to avoid EMC problems. In addition, PESDXL4UW/TVSX4 connected to SIM track is to avoid ESD problem.

To implement SIM detection function, a resistor is required to add to the trace of PIN5. You need to select a SIM holder with the detection pin.

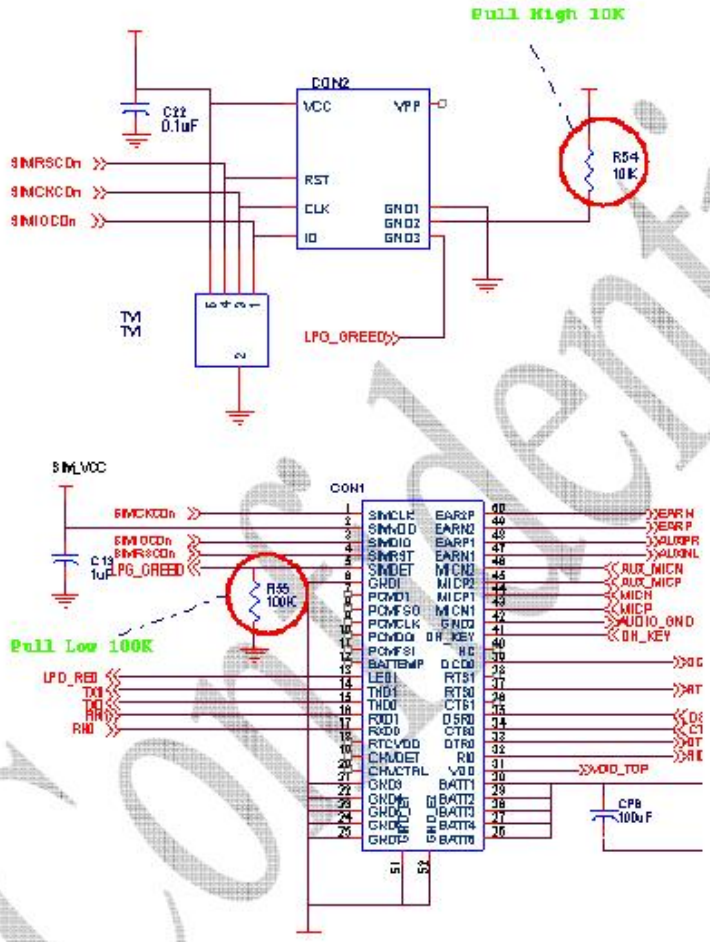


Figure 11: Reference circuit for SIM interface

4.3.2 SIM Layout

It's important to pay additional caution to the ESD component of SIM connector layout. Following are suggested guidelines for the layout of SIM holder.

1. The ESD component should be placed as close as possible to the SIM connector.

2. The ESD component should be connected to a clean ground to perform well.
3. Track between ESD to SIM connector should be 8mil wide.
4. Each signal track of SIM circuit needs to be surrounded by ground.
5. Tracks distance between SIM connector and GSM module connector should be below 10 cm.

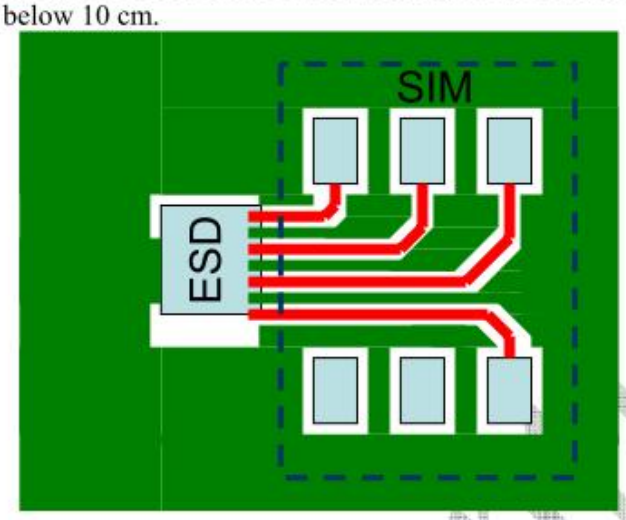


Figure 12: SIM connector layout reference

4.3.3 SIM Card Interface

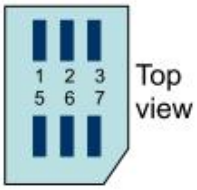


Table 6: SIM connector pin out

Pin number	Schematics name	Description
1	SIM_VCC	Supply voltage (1.8 or 3V)
2	SIMRSCDn_ESD	Reset for SIM card
3	SIMCKCDn_ESD	Clock for SIM card
5	GND	Ground
6	SIM_VCC	Supply voltage (1.8 or 3V)
7	SIMIOCD_ESD	I/O line to/from SIM card

4.4 RF interface

When the antenna is connected to the module through a 50Ω coaxial cable, the coaxial cable must be connected to both the "Antenna pad" and the "Ground pad".
It is recommended to use an RG178 coaxial cable with the following stripping and mounting guidelines. User needs to select RF cable with minimum signal loss at GSM 850/E-GSM 900Mhz and DCS 1800/PCS 1900Mhz.

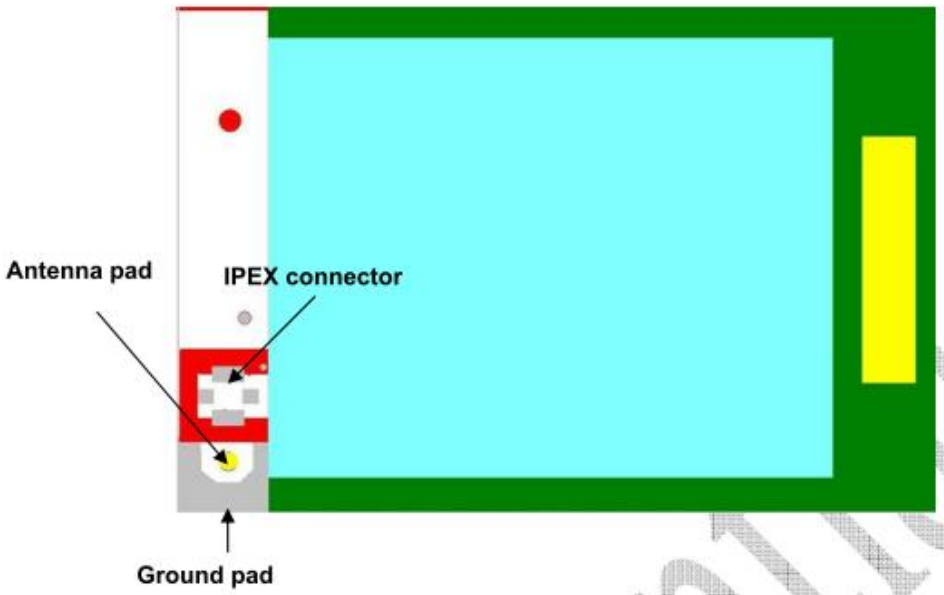


Figure 13: RF interface

4.5LED Indicators

PIN 5 and PIN 13 can be used as system indicators (refer to enhanced AT command for function switch):

PIN 5: When the output is at high level, the system is ready to accept AT command.

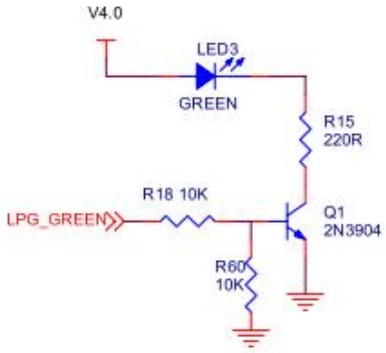


Figure 14: PIN 5 for system ready indication

PIN 13: When the output is at high level, the module had camped on the network.

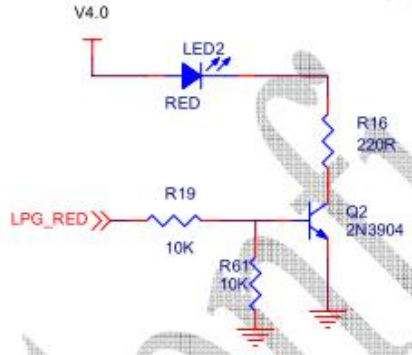


Figure 15: PIN 13 for network ready indication

5. Power ON/OFF Procedure

ON_KEY: used for Power ON/OFF and this pin is active low. Please refer to the recommended circuit below.

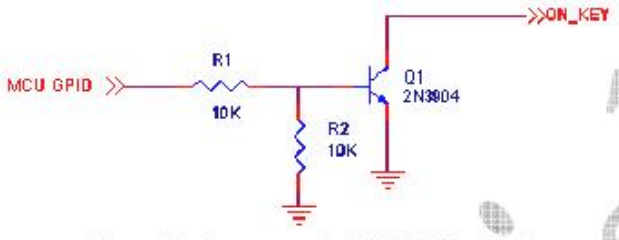


Figure 16: Recommended ON_KEY circuit

Power ON:

- Prior to system power on, ON_KEY, CTS and DSR need to be high. After the system is powered on, wait for approximately 200 ms and then pull the ON_KEY level to low for 2 seconds to perform system power on procedures.
- To start the communication with the module, ON_KEY needs to be pulled back to high. Wait for 200 ms and then pull CTS and DSR level to low simultaneously. Then, communication through UART0 can begin.

Power OFF:

- Prior to powering off the system, it is required to pull CTS and DSR levels back to high. Wait for approximately 200 ms and then pull the ON_KEY level to low for 2 seconds. Wait for another 200 ms interval before proceeding to system power off procedure.

The voltage levels mentioned above are in terms of the module itself. In other words, if it is the MCU that passes through the circuit above, the levels need to be reversed. It is required to have an interval of 3.4 seconds between Power ON and Power OFF.

Thus it is recommended to use the following procedure to power on/off module (figure 14 to 15).

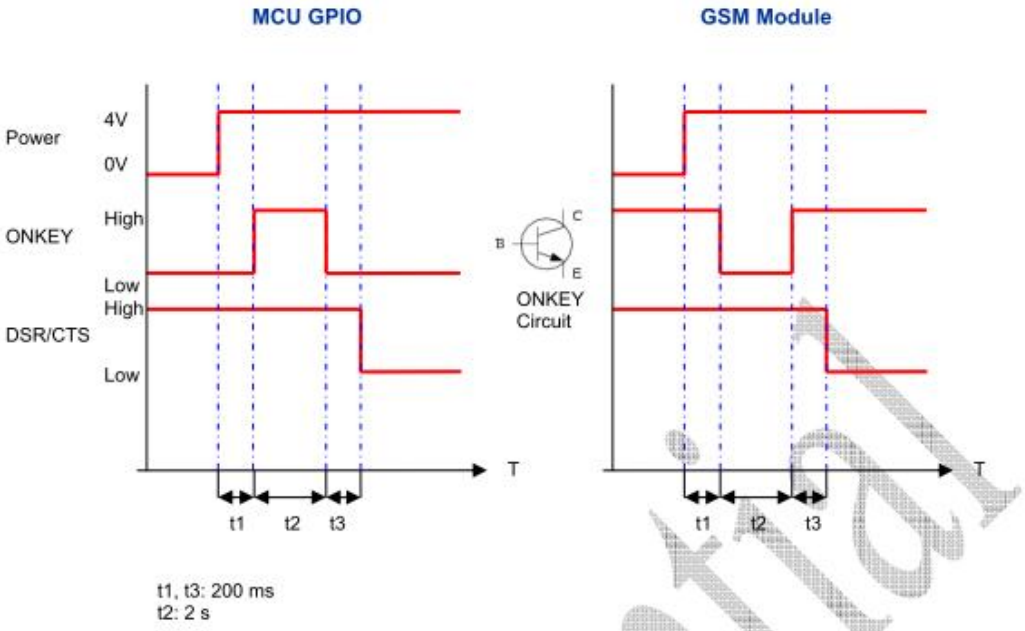


Figure 17: Power ON sequence

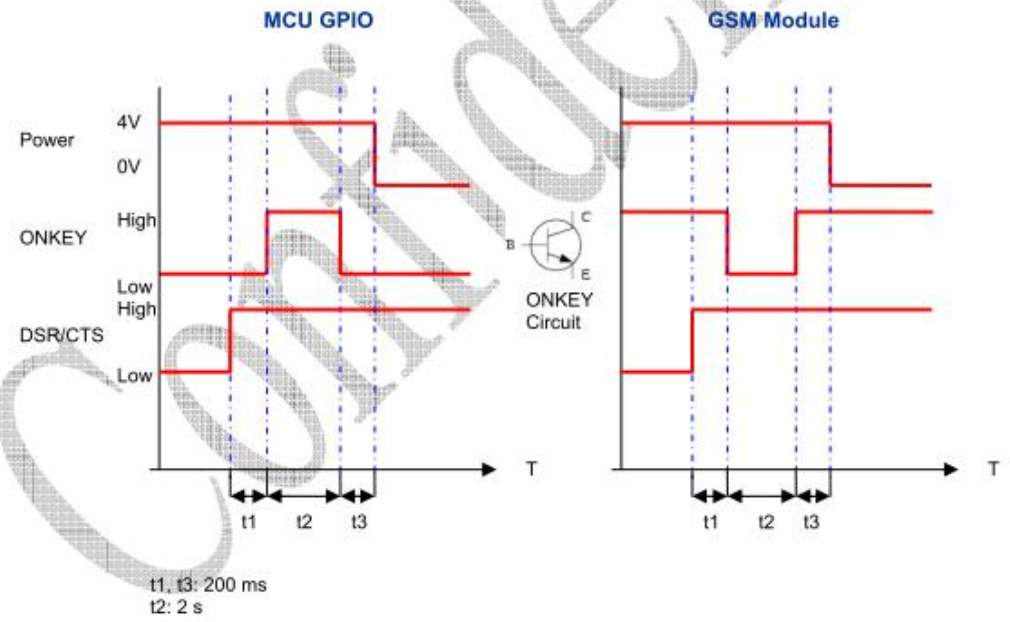


Figure 18: Power OFF sequence

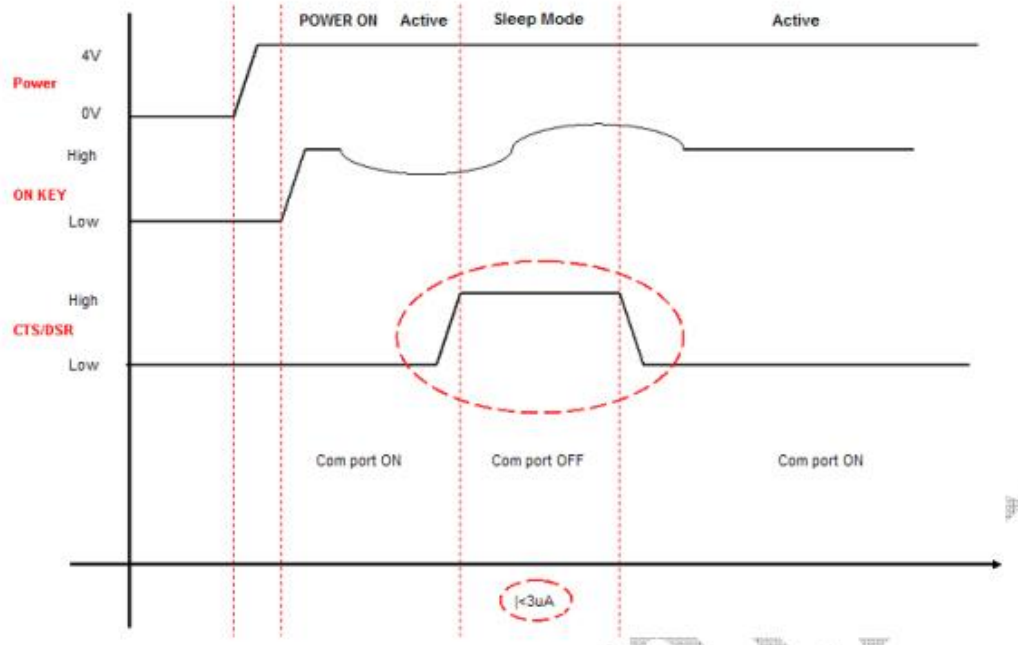


Figure 19: GSM Sleep Process

Electrical & Environmental Characteristics

Table 7: MIC 1 audio input electrical requirements

Parameter	Typical Value
Maximum input level (MIC+–MIC-)	32.5mVrms
Differential input resistance (MICI+–MICI-)	220 KΩ
MIC Skew voltage	1.9~2.1V
	2.0~2.2V

Table 8: MIC1 audio output electrical information

Parameter	Testing condition	MIN	TYP	MAX
Resistance (MIC+–MIC-)	4VPP Output	16Ω	-	-
	3V 1KHz	<1Ω	-	-

Table 9: EAR 1 audio output electrical information

Parameter	Testing condition	MIN	TYP	MAX
EAR+ or EAR- maximum capacitance differential	Differentiate 4VPP	-	-	1%
EAR+ or EAR- maximum output	16Ω 5%	3.1VPP	-	43.92VPP
	4Ω 5%	1.2VPP	-	1.5VPP

Table 10: EAR2 audio output electrical information

Parameter	Testing condition	MIN	TYP	MAX
EAR+ or EAR- capacitance differential	Differential 4VPP	-	-	1%
EAR+ or EAR- maximum output	16Ω 5%	3.1VPP	-	43.92VPP
	4Ω 5%	1.2VPP	-	1.5VPP

Table 11: Input power requirement

Parameter	Min	Typ	Max	Unit
VBat+	3.4	4.0	4.5	V

Table 12: Operation current requirement

Operation mode	Min	TYP	Max	Unit
Standby mode	-	-	2	mA
Talking mode	-	250	-	mA
GPRS data transmission	-	350(GPRS4+1)	-	mA
Power off mode	-		100	μA

Appendix 1. Summary of Pin Out

The board to board connection pin definitions of ADH8066 are described as below table:

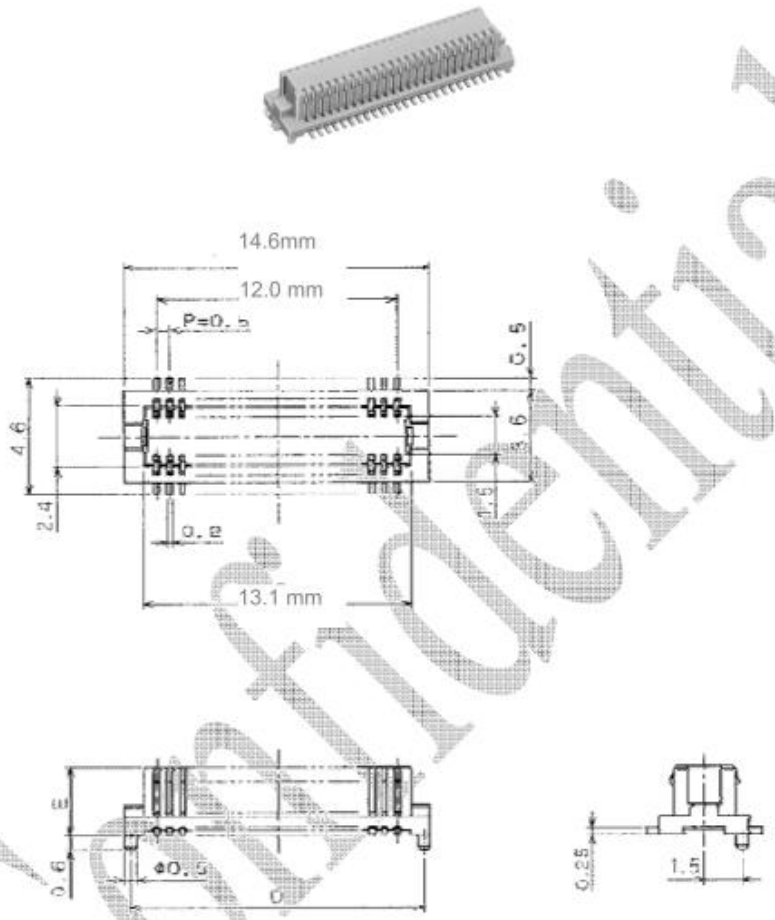
PIN.NO	PIN.NAME	Note
1	SIMCLK	SIM Card interface, supporting 1.8V/3V SIM card
2	SIMVDD	
3	SIMIO	
4	SIMRST	
5	GPIO10	Default as ready for AT COMMAND, can be used as SIM detector
6	GND	Ground
7	PCMDI	PCM data input
8	PCMFSO	PCM frame synchronization
9	PCMCLK	PCM clk
10	PCMDO	PCM data output
11	ADC1	Adc1
12	BATTEMP	Adc2 (bat temp)
13	GPIO3	Default as GSM network indicator
14	TXD1	UART1 Data Output
15	TXD0	UART0 Data Output
16	RXD1	UART1 Data Input
17	RXD0	UART0 Data Input
18	VCHAGE	Charging interrupt detection, also can be used as charging pin with current limit under 400Ma.
19	VCHAGE	Charging interrupt detection, also can be used as charging pin with current limit under 400Ma.
20	CHV_DRV	CHV_DRV charging control
21	GND	Ground
22	GND	
23	GND	
24	GND	
25	GND	
26	VBAT	Power input positive, input voltage is limited to 3.5V~4.5V.
27	VBAT	
28	VBAT	
29	VBAT	
30	VBAT	
31	V1.8	1.8V Power output with load of 50mA
32	RI0	UART0 ring tone indicator output, can also be used as GPIO or interrupt.
33	DTR0	UART0 Ready to receive, can be used as GPIO
34	CTS0	UART0 Permission to sent

35	DSR0	UART0 Ready to receive, can be used as GPIO or interrupt
36	IICSCL	NC
37	RTS0	UART0 Request to send (Output)
38	IICSDA	NC
39	DCD0	UART0
40	CHV_MAX	NC
41	ON_KEY	Power On/OFF signal. Effective at low. Required 100ms above power level
42	GND	
43	MIC1_P	Mic 1 in positive
44	MIC1_N	Mic 1 in negative
45	MIC2_P	Mic 2 in positive
46	MIC2_N	Mic 2 in negative
47	AUXOUTP	AUX out 2 positive
48	AUXOUTN	AUX out 2 negative
49	EARP	Audio out 1 positive
50	EARN	Audio out 1 negative

Appendix 2. Board to Board connector dimension

ADH8066 connector is a 50 Pin Board to Board connector with 0.5mm pitch as pig 2-1. The model number is Hirose's DF12C(3.0)-50DS-0.5V. The connector is as figure 14.

Figure 20: 50 pin board to board connector



Appendix 3. Antenna Connector

Antenna interface of ADH8066 is GSC RF connector to be connected with an external antenna cable to the module. ADH8066 uses an ultra-miniature SMT antenna (Model Name: U.FL-R-SMT) connector from Hirose Ltd. The physical dimension of antenna connector is described in below figure.

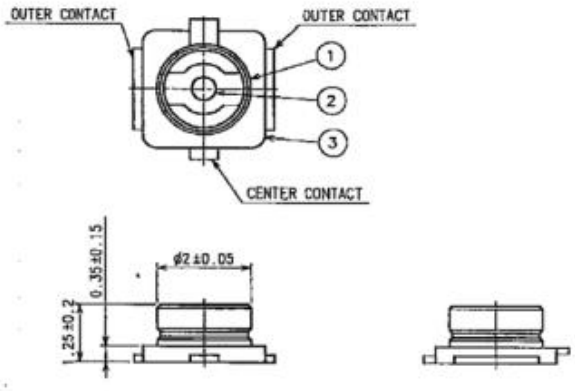


Figure 21: RF antenna connector