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Spartan 3E Evaluation Card DataSheet

Spartan 3E Breakout

The Spartan 3E Evaluation Card consists of two parts, a breakout with almost all I/Os undedicated, and a support area. If the user would like to use the breakout board in their own project, they can shear the two sections apart at the partition.

Breakout Module

The module is a direct breakout of the XC3S500E-PQG208 device mounted in the center of it, along with decoupling caps. Power supply rails are tied together, along with the individual bank VCCOs. The bank VCCOs are on separate rails to permit different I/O standards to be used. The only I/O pin that is dedicated is the IO_L16N_O/HSWAP IO, on pin 206, which is tied to ground on Rev 2.1 boards.

Support Module

The support module contains three fixed voltage regulators set at 1.2, 2.5 and 3.3 V, to be used with VCCCORE, VCCAUX and optionally the VCCOs. Each regulator is separated from the support board circuitry via a jumper [Block A], to allow for user supplied power supplies to be used to power the board. Also present are 4 jumpers to tie each VCCO bank separately to 3.3V [Block B]. These jumpers should be present for normal operation. If a bank is not tied to 3.3V for VCCO, an alternate acceptable power supply should be provided.

Also present on the support module are an RS/232 level shifter, and a 16Mbit SPI PROM. The level shifter is connected to the FPGA via jumpers [Block C] to allow the pins connected to it to be used for other purposes. The PROM is used to boot the FPGA when Master SPI mode is selected. There is space available in the PROM for other user data after the FPGA configuration image.

Programming / Configuration

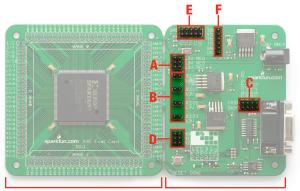
Programming of the FPGA can be done through either of the JTAG ports onboard. The 2x5 header [Block E] is intended for a SparkFun parallel port programmer, and the 1x6 header is provided for a Digilent programmer [Block F]. The default configuration mode of the board is set via the M0-M2 jumpers [Block D]. A legend on the board indicates which jumpers need to be set for which mode. See the Spartan 3E user guide for

more information on configuration modes at http://www.xilinx.com/xlnx/xweb/xil publications display.jsp?category=-1211393.

Programming the SPI PROM can be done using ImpactTM included with Xilinx Webpack, or for users with an older version of Webpack, or for those who cannot use Impact, a python is script available on the Spartan 3E Evaluation Card product page on the SparkFun website.

Known Errata

R2.1: Silk screen pin labels for SparkFun JTAG connector has TMS and TD0 swapped. The actual pinout itself is correct with regards to the SparkFun Xilinx Programmer.



Breakout Module

Support Module

ROHS PB

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