SPECIFICATION

MODULE NO	NL128128C-EIF
VERSION	VER.0
CUSTOMER	
APPROVED	

Approved	Checked	Prepared

科創光電股份有限公司
台中市北屯區北屯路 360 號 7 樓之一
NewTec Display Co., Ltd.
7F-1, No360, Beitun Rd., Taichung City 406, Taiwan (R.O.C.)
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http://www.newtec.com.tw

INDEX

ISSUE RECORD

Module NO.		
DATE	Version	Description
09/01/19	0	Published

1.Numbering system

N L 128128 C – E –
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

1 .Brand Name

N	NEWTEC Display Co., LTD

2. Display Type

T	TAB
B	Graphic
C	Character
O	COG
R	Color-STN
S	Seven-Segment
L	OLED

3. Number of Pixels

Character Module	Characters per line × Lines
Graphic Module	Row Dots × Column Dots

4. Series number

A~Z	Series Number

5. LCD Mode:

	TN	STN		FSTN	Color-STN	OLED
Positive	T	G	Gary	F	R	E (Green)
		Y	Yellow/Green			
Negative	N	B	Blue	M		

6. LCD Polarize

	Normal Temperature				Wide Temperature			
	6:00	12:00	3:00	9:00	6:00	12:00	3:00	9:00
Reflective	A	D	M	P	G	J	S	V
Transflective	B	E	N	Q	H	K	T	W
Transmissive	C	F	O	R	I	L	U	X
Y: Other(Normal temperature and wide viewing angle)								

7. OLED color

B	Blue

G	Green
R	Red
F	Full Color
Y	Yellow

8. IC font (Character)

Cyrillic/English	TS,TP
Chinese/English	C(BIG 5), S(GB)
Japanese/English	PN,PS,PM,PP
European/English	RN,RS,RK,RP

9. Special code

A	Anti-glare
H	Touch panel
M	Negative voltage output and temperature compensation on board
N	With negative voltage output on board
X	Without negative voltage output on board

10. Others

1.2 Precaution in use of OLED Module

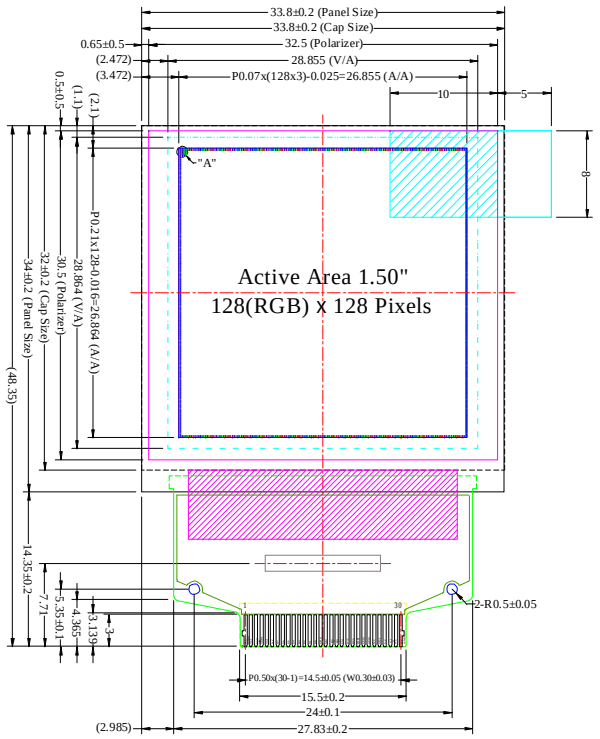
(1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
(2) Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
(3) Don't disassemble the OLED.
(4) Don't operate it above the absolute maximum rating.
(5) Don't drop, bend or twist OLED.
(6) Soldering: only to the I/O terminals.
(7) Storage: please storage in anti-static electricity container and clean environment.
(8) Don't touch the elastomer connecter, especially insert a backlight panel (EL or CCFL)

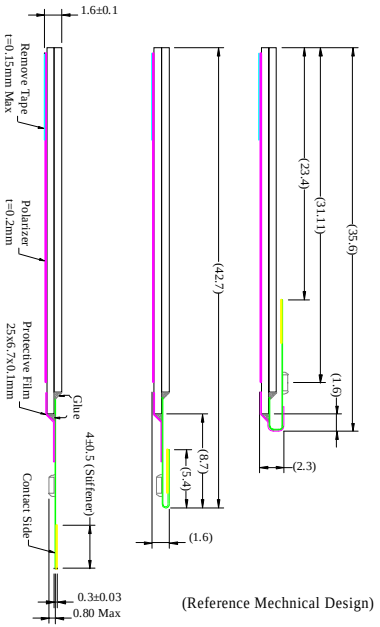
1.3 General Specification

Mechanical Dimension

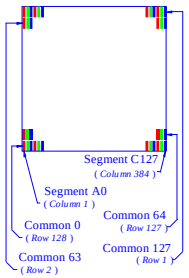
Item	Dimension	Unit
Number of Characters	128(RGB) x128	—
Panel Size	33.80 x 34.00 x 1.60	mm
Active area	26.855 x 26.864	mm
Pixel size	0.045 x 0.194	mm
Pixel pitch	0.07 x 0.21	mm

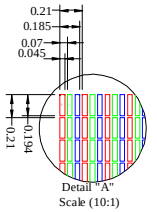
Item	Date	Remark
A	20080815	Original Drawing





(Reference Mechnical Design)





Pin	Symbol
1	N.C. (GND)
2	VCC
3	VCOMH
4	VDDIO
5	VSL
6	N.C.
7	D7
8	D6
9	D5
10	D4
11	D3
12	D2
13	D1
14	D0
15	E/RD#
16	R/W#
17	BS0
18	BS1
19	CS#
20	D/C#
21	RES#
22	IREF
23	GPIO1
24	GPIO0
25	N.C.
26	VDD
27	VCI
28	VSS
29	N.C.
30	N.C. (GND)

Notes:

1. Driver IC: SSD1351
2. Die Size: 10700um x 1500um
3. COF Number: SSD1351U3
4. Interface:
   8-bits 68XX/80XX Parallel, 3-/4-wire SPI
5. General Tolerance: ±0.30
6. The total thickness (1.70 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.95 Max.

Customer Approval Signature	NEWTEC DISPLAY					Drawing Number	Rev.
						DFE2828CNCF38	A
	Unless Otherwise Specified		Title	Folding Type OEL Display Module Pixel Number: 128(RGB) x 128, 262144 Colors, COF Package		Material	
	Unit	mm				Soda Lime / Polyimide	
	General Roughness						
	Tolerance			Drawn	E.E.	Panel / E.	P.M.
	Dimension	±0.3	By	Humphrey Lin	Sean Lai	Ivy Lo	Cherry Lin
	Angle	±1	Date	20080815	20080815	20080815	20080815

Scale	Sheet	Size
1:1	1 of 1	A3

1.5 Pin Definition

Pin Number	Symbol	Type	Function
Power Supply			
27	VCI	P	*Power Supply for Operation* This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
26	VDD	P	*Power Supply for Core Logic Circuit* This is a voltage supply pin which is regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
4	VDDIO	P	*Power Supply for I/O Pin* This pin is a power supply pin of I/O buffer. It should be connected to VCI or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pul high, they should be connected to VDDIO.
28	VSS	P	*Ground of OEL System* This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
2	VCC	P	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. It must be connected to external source.
Driver			
22	IREF	I	*CurrentReferencefor Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5uA.
3	VCOMH	P	*VoltageOutputHigh Level forCOM Signal* This pin is the input pin for the voltage output high level for COM A tantalum capacitor should connected between this pin and VSS.
5	VSL	P	*VoltageOutputLow Level for SEG Signal* This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
External IC Control			
24 23	GPIO0 GPIO1	I/O	*General PurposeInput/Output* These pins could be left open individually or have signal inputted/outputted. They are able to use as the external DC/DC converter circuit enabled/disabled control or other applications.

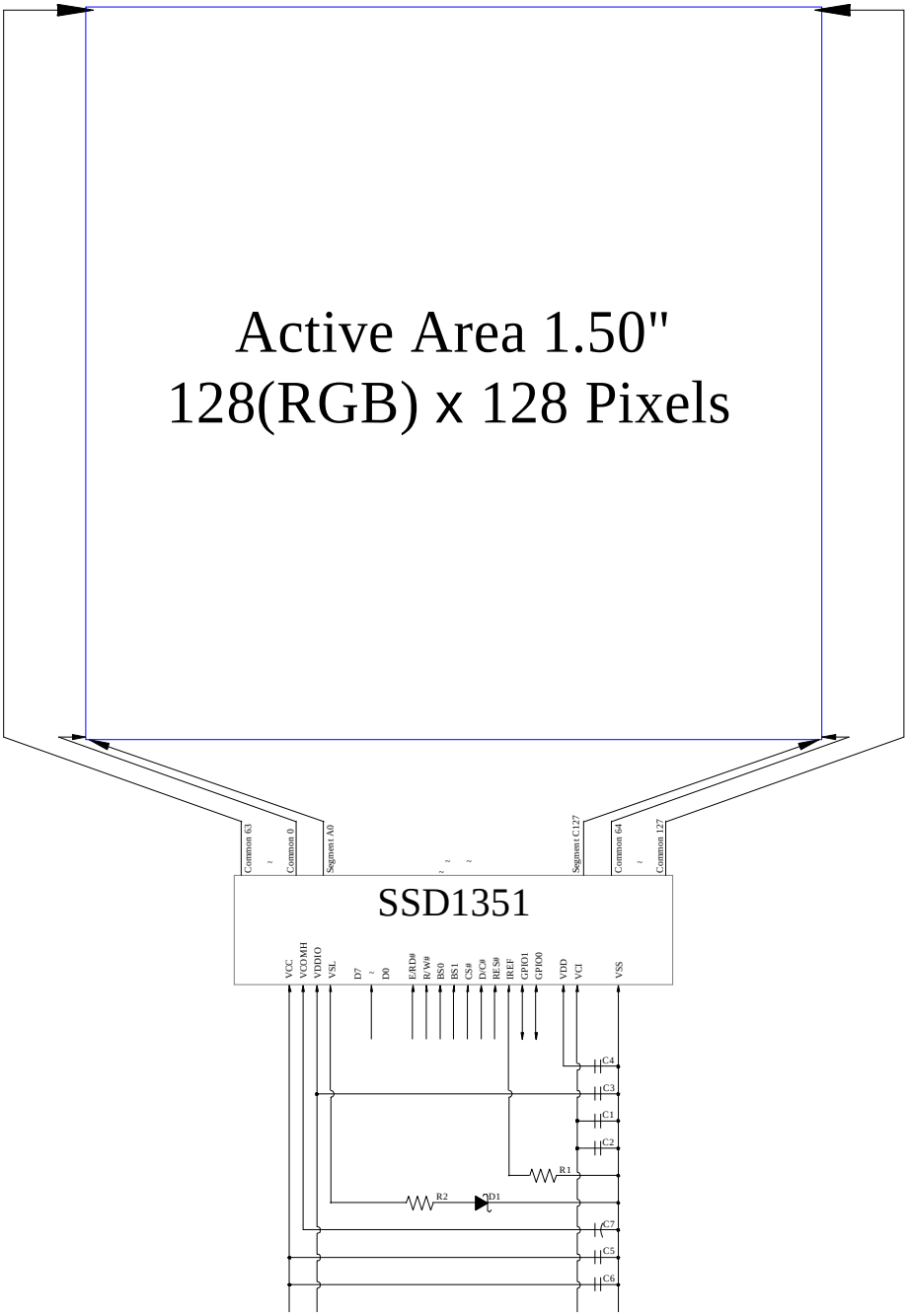
1.5

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>17
18</td><td>BS0
BS1</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td></tr>
<tr><td>68XX-parallel (8-bit)</td><td>1</td><td>1</td></tr>
<tr><td>80XX-parallel (8-bit)</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>21</td><td>RES#</td><td>I</td><td>Power Reset forControllerand Driver
This pin is reset signal When the pin is initialization of the chip is executed.</td></tr>
<tr><td>19</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>20</td><td>D/C#</td><td>I</td><td>Data/CommandControl
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When 3-wire serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>15</td><td>E/RD#</td><td>I</td><td>Read/Write Enableor Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal.Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16</td><td>R/W#</td><td>I</td><td>Read/Write Selector Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor,this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS.</td></tr>
<tr><td>7~14</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
Unused pins must be connected to VSS except for D2.</td></tr>
</table>

1.5

Pin Number	Symbol	I/O	Function
Reserve			
6, 25, 29	N.C.	-	*Reserved Pin* The N.C. pins between function pins are reserved for compatible and flexible design.
1, 30	N.C. (GND)	-	*Reserved Pin(SupportingPin)* The supporting pins can reduce the influences from stresses on the function These pins must be connected to external ground.

1.6 Block Diagram



MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#

C1, C5: 0.1µF
C2: 4.7µF
C6: 10µF
C3, C4: 1µF
C7: 4.7uF / 25V Tantalum Capacitor
R1: 560kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

2.

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics" .If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3.

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	With Polarizer (Note 3)	70	90	-	cd/m^2
C.I.E. (White)	(x) (y)	With Polarizer	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	With Polarizer	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	With Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	With Polarizer	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 13V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	12.5	13	13.5	V
High Level Input	V_{IH}		$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2\times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100µA, 3.3MHz	$0.9\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100µA, 3.3MHz	0	-	$0.1\times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	240	300	µA
Operating Current for V_{CC}	I_{CC}	Note 4	-	23.2	29.0	mA
		Note 5	-	33.4	41.8	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	µA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	µA

Note 3: Brightness and Supply Voltage for (V_{CC}) are to change of the panel characteristics and the customer's request.
Note 4: V_{CI} = 2.8V, V_{CC} = 13V, 50% Display Area Turn on.
Note 5: V_{CI} = 2.8V, V_{CC} = 13V, 100% Display Area Turn on.

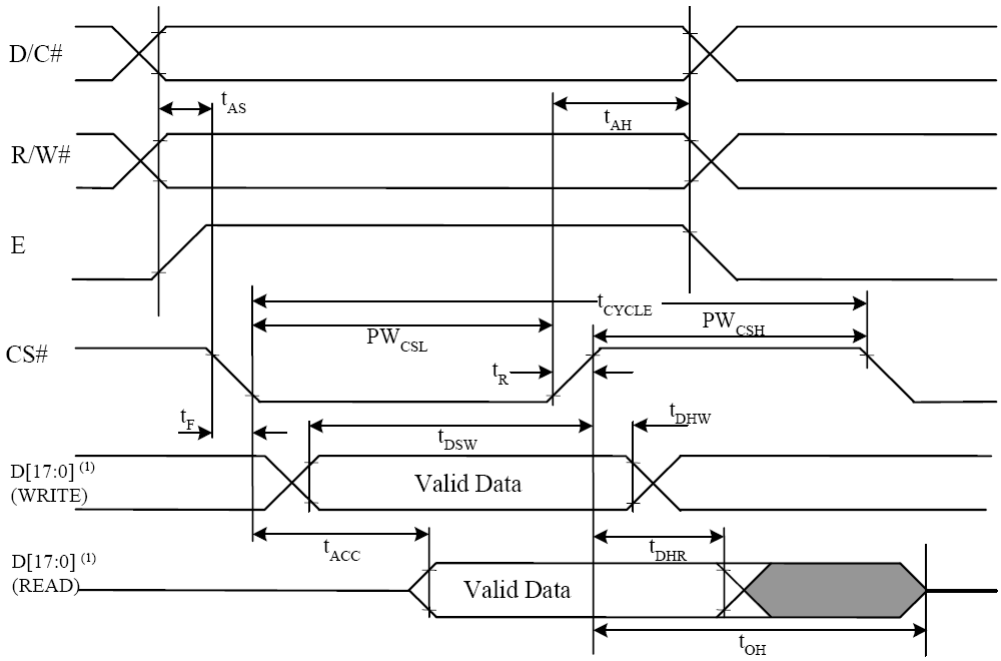
* Software configuration follows Section 4.4 Initialization.

3.3

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 2.8V, T_a = 25°C

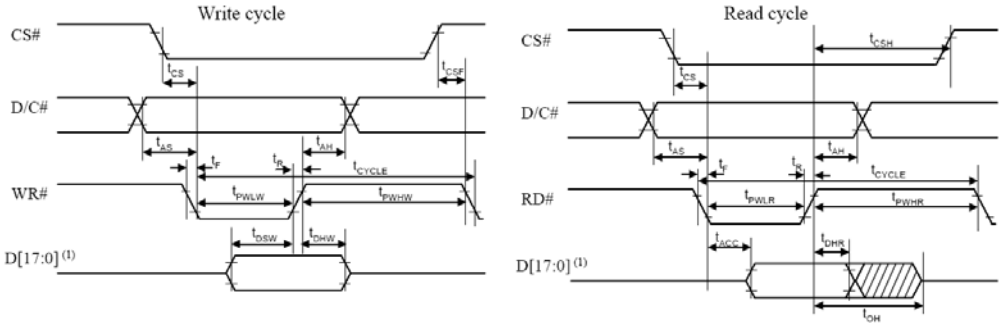


* (1) When 8-bit Used: D[7:0] Instead

3.3.2

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 2.8V, T_a = 25°C)

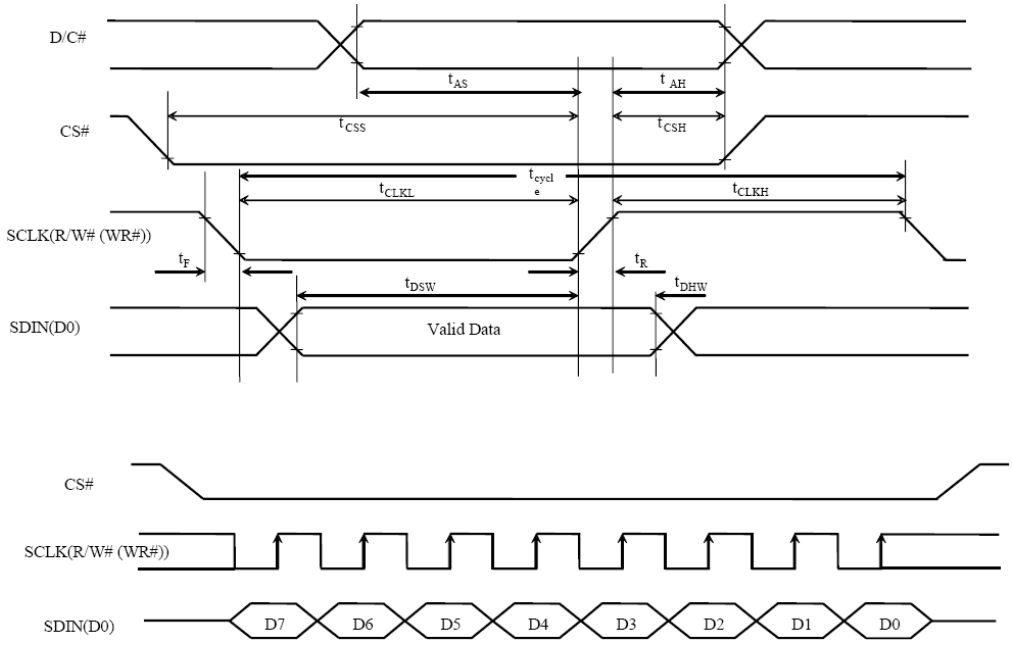


* (1) When 8-bit Used: D[7:0] Instead

3.3.3

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

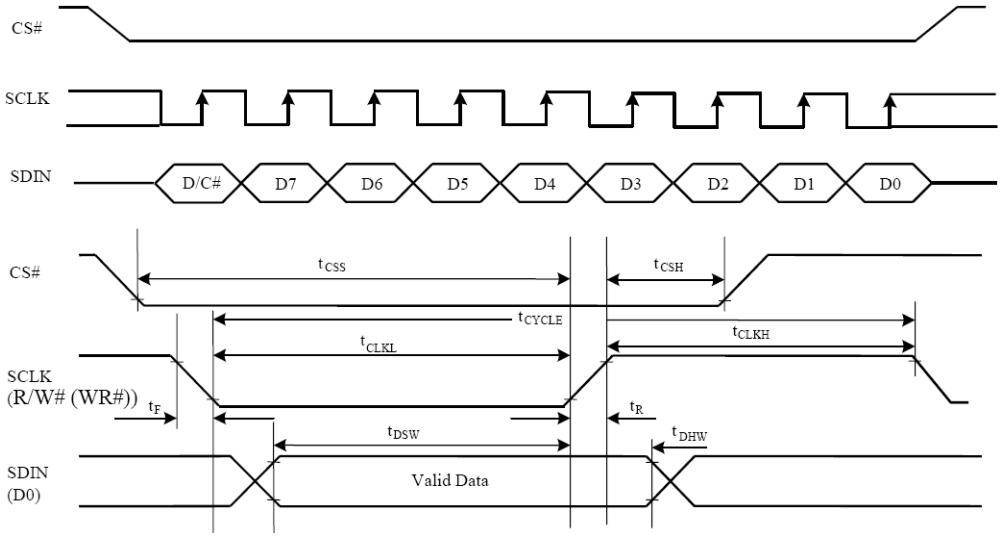
* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 2.8V, T_a = 25°C)



3.3.4

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.65V, V_{CI} = 2.8V, T_a = 25°C)



4.

4.1. Commands

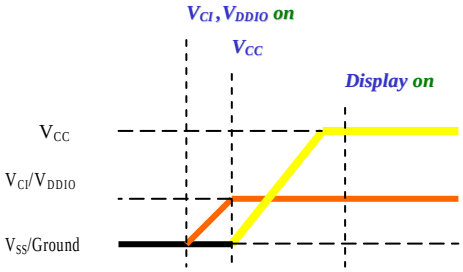
Refer to the Technical Manual for the SSD1351

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

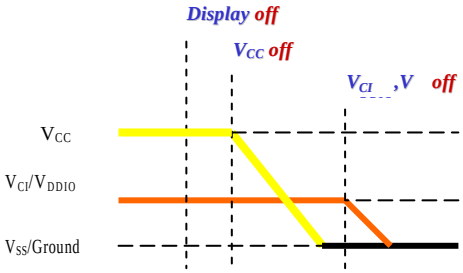
4.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (when V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



4.3 Reset Circuit

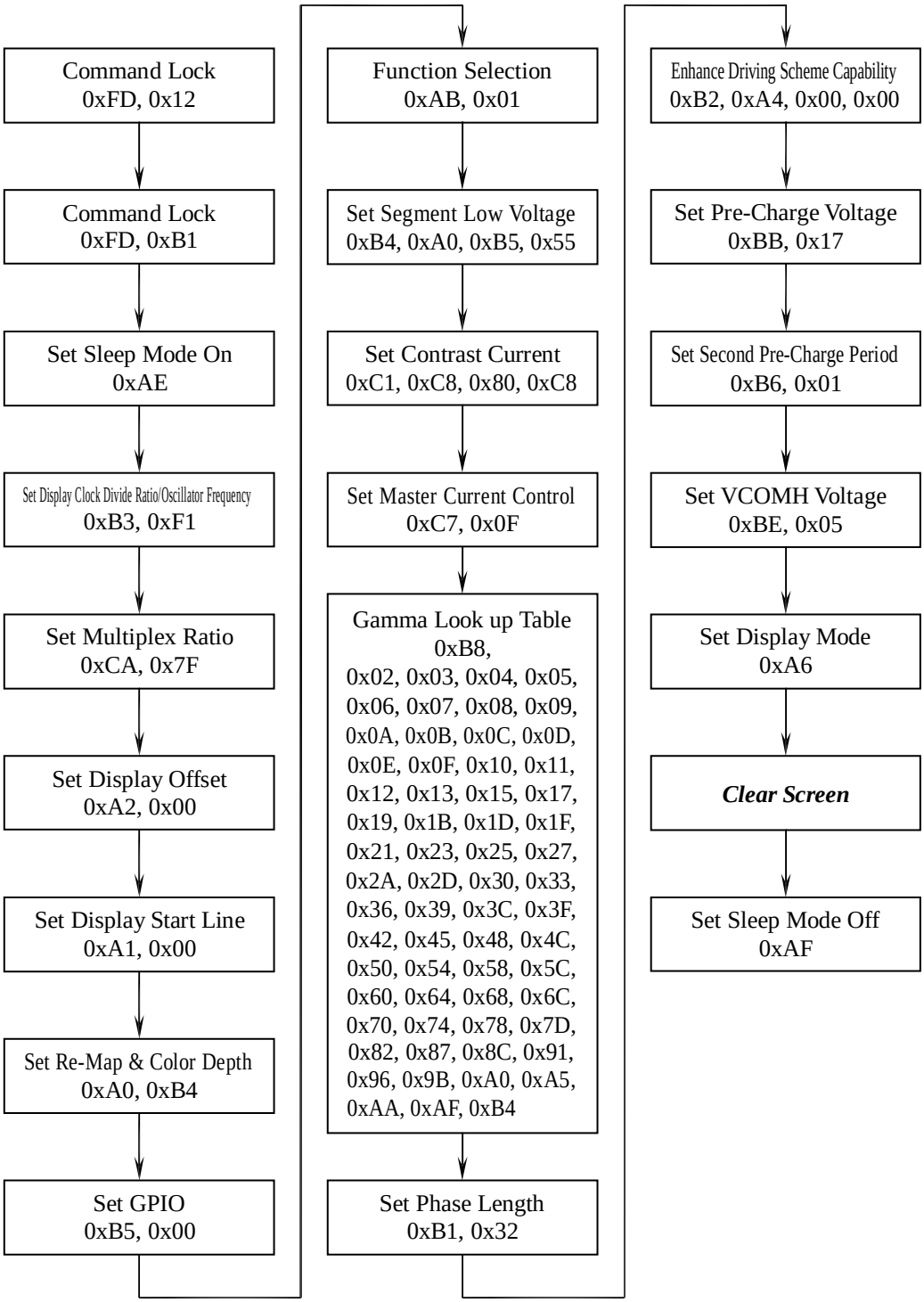
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128(RGB)×128 Display Mode
3. Normal segment and display data column and row address (SEG0 mapping
4. mapped to column address 00h and COM0 mapped to row address 00h)
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	90 cd/m^2, 50% Checkerboard	6
Storage Life Time	20,000	-	hr	T_a = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimat by the

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality ControlSpecifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

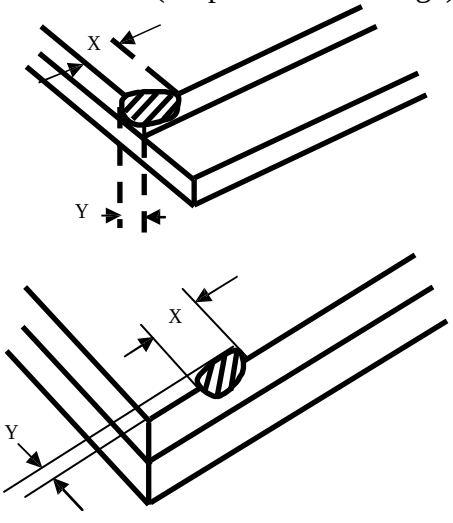
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

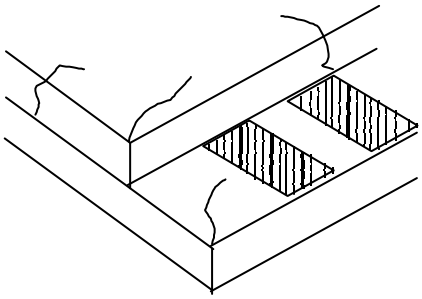
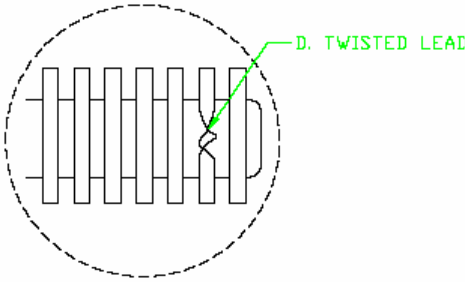
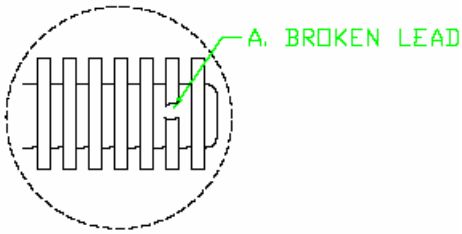
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

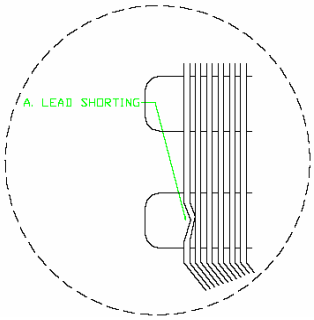
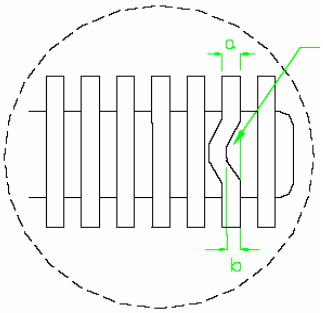
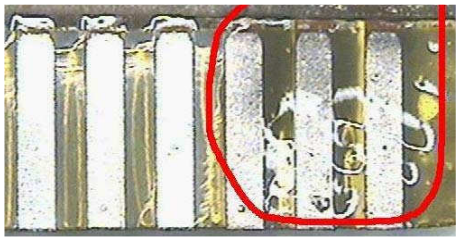
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

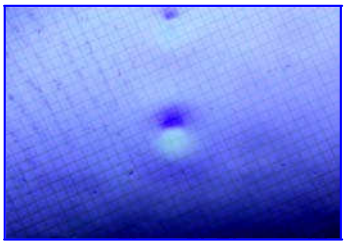
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	 Not Allowable
Terminal Lead Twist	Minor	
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
Glue or Contamination on Pin (~~Couldn't Be Removed~~ by Alcohol)	Minor	NG for horizontally bent lead more than 50% of its width. 
Ink Marking on Back Side of panel (Exclude on Film)	Minor	
	Acceptable	Ignore for Any

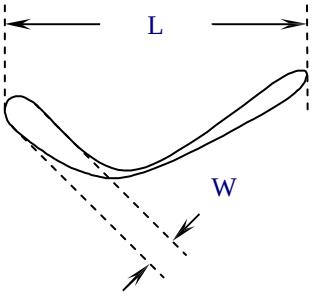
6.3.2 Cosmetic Check (Display Off) in Active Area

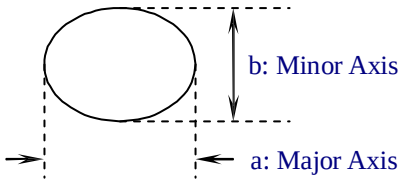
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1, L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Spot-Shape Defect (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 <Φ ≤ 0.25 n ≤ 1 0.25 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not allowable

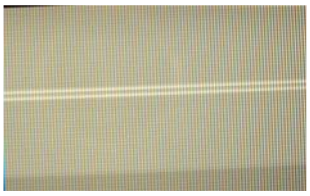
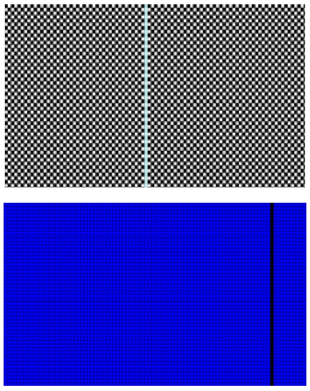
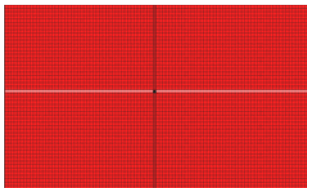
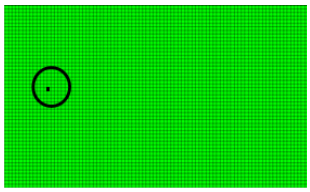
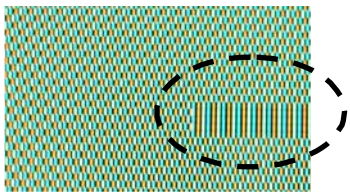
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not allowable
Bright Line	Major	
Missed Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major