The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output enable (\(G\)) is held high, all data in the output buffers is held low and all drain outputs are off. When \(G\) is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at \(T_C = 25^\circ C\). The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B595 is characterized for operation over the operating case temperature range of \(-40^\circ C\) to \(125^\circ C\).
logic diagram (positive logic)
schematic of inputs and outputs

**EQUIVALENT OF EACH INPUT**

- **VCC**
- Input
- **GND**
- **25 V**
- **12 V**

**TYPICAL OF ALL DRAIN OUTPUTS**

- **DRAIN**
- **50 V**
- **20 V**
- **GND**

**absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†**

- Logic supply voltage, \( V_{CC} \) (see Note 1) .......................................................... 7 V
- Logic input voltage range, \( V_I \) .......................................................... –0.3 V to 7 V
- Power DMOS drain-to-source voltage, \( V_{DS} \) (see Note 2) ........................................ 50 V
- Continuous source-to-drain diode anode current ........................................ 500 mA
- Pulsed source-to-drain diode anode current (see Note 3) .......................... 1 A
- Pulsed drain current, each output, all outputs on, \( I_D, T_C = 25°C \) (see Note 3) ............. 500 mA
- Continuous drain current, each output, all outputs on, \( I_D, T_C = 25°C \) .......... 150 mA
- Peak drain current single output, \( I_{DM}, T_C = 25°C \) (see Note 3) ...................... 500 mA
- Single-pulse avalanche energy, \( E_{AS} \) (see Figure 4) .................. 30 mJ
- Avalanche current, \( I_{AS} \) (see Note 4) .................................................. 500 mA
- Continuous total dissipation ........................................................................ See Dissipation Rating Table
- Operating virtual junction temperature range, \( T_J \) .................................. –40°C to 150°C
- Operating case temperature range, \( T_C \) ........................................ –40°C to 125°C
- Storage temperature range ........................................................................ –65°C to 150°C
- Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds ....... 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**NOTES:**

1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
4. DRAIN supply voltage = 15 V, starting junction temperature (\( T_{JS} \)) = 25°C, \( L = 200 \text{ mH} \), \( I_{AS} = 0.5 \text{ A} \) (see Figure 4).

**DISSIPATION RATING TABLE**

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>( T_C \leq 25°C ) POWER RATING</th>
<th>DERATING FACTOR ABOVE ( T_C = 25°C )</th>
<th>( T_C = 125°C ) POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>DW</td>
<td>1389 mW</td>
<td>11.1 mW/°C</td>
<td>278 mW</td>
</tr>
<tr>
<td>N</td>
<td>1050 mW</td>
<td>10.5 mW/°C</td>
<td>263 mW</td>
</tr>
</tbody>
</table>
### recommended operating conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic supply voltage, VCC</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, V_{IH}</td>
<td>0.85</td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>Low-level input voltage, V_{IL}</td>
<td>0.15</td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>Pulsed drain output current, T_{C} = 25°C, V_{CC} = 5 V (see Notes 3 and 5)</td>
<td>−500</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>Setup time, SER IN high before SRCK↑, t_{SU} (see Figure 2)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hold time, SER IN high after SRCK↑, t_{H} (see Figure 2)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse duration, t_{w} (see Figure 2)</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Operating case temperature, T_{C}</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### electrical characteristics, V_{CC} = 5 V, T_{C} = 25°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(BR)DSX, Drain-to-source breakdown voltage</td>
<td>ID = 1 mA</td>
<td>50</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{SD}, Source-to-drain diode forward voltage</td>
<td>IF = 100 mA</td>
<td>0.85</td>
<td>1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OH}, High-level output voltage, SER OUT</td>
<td>IOH = −20 μA, V_{CC} = 4.5 V</td>
<td>4.4</td>
<td>4.49</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IOH = −4 mA, V_{CC} = 4.5 V</td>
<td>4</td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OL}, Low-level output voltage, SER OUT</td>
<td>IOL = 20 μA, V_{CC} = 4.5 V</td>
<td>0.005</td>
<td>0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IOL = 4 mA, V_{CC} = 4.5 V</td>
<td>0.3</td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IH}, High-level input current</td>
<td>V_{CC} = 5.5 V, V_{I} = V_{CC}</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>I_{IL}, Low-level input current</td>
<td>V_{CC} = 5.5 V, V_{I} = 0</td>
<td>−1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>ICC, Logic supply current</td>
<td>V_{CC} = 5.5 V</td>
<td>20</td>
<td>100</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>All outputs off</td>
<td>150</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC(FRQ), Logic supply current at frequency</td>
<td>ISRCK = 5 MHz, C_{L} = 30 pF, All outputs off, See Figures 2 and 6</td>
<td>0.4</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_N, Nominal current</td>
<td>V_{DS(on)} = 0.5 V, I_N = ID, T_{C} = 85°C</td>
<td>90</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>See Notes 5, 6, and 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{DSX}, Off-state drain current</td>
<td>V_{DS} = 40 V, V_{CC} = 5.5 V</td>
<td>0.1</td>
<td>5</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_{DS} = 40 V, V_{CC} = 5.5 V, T_{C} = 125°C</td>
<td>0.15</td>
<td>8</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>r_{DS(on)}, Static drain-source on-state resistance</td>
<td>ID = 100 mA, V_{CC} = 4.5 V</td>
<td>4.2</td>
<td>5.7</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ID = 100 mA, V_{CC} = 4.5 V, T_{C} = 125°C</td>
<td>6.8</td>
<td>9.5</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ID = 350 mA, V_{CC} = 4.5 V</td>
<td>5.5</td>
<td>8</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
3. Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
5. Technique should limit T_{J} − T_{C} to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_{C} = 85°C.
swtiching characteristics, \( V_{CC} = 5 \text{ V}, T_C = 25^\circ \text{C} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation delay time, low-to-high-level output from ( G )</td>
<td>( C_L = 30 \text{ pF}, I_D = 100 \text{ mA} ), See Figures 1, 2, and 9</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation delay time, high-to-low-level output from ( G )</td>
<td>( C_L = 30 \text{ pF}, I_D = 100 \text{ mA} ), See Figures 1, 2, and 9</td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_r )</td>
<td>Rise time, drain output</td>
<td>( C_L = 30 \text{ pF}, I_D = 100 \text{ mA} ), See Figures 1, 2, and 9</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_f )</td>
<td>Fall time, drain output</td>
<td>( C_L = 30 \text{ pF}, I_D = 100 \text{ mA} ), See Figures 1, 2, and 9</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{a} )</td>
<td>Reverse-recovery-current rise time</td>
<td>( I_F = 100 \text{ mA}, di/dt = 20 \text{ A/μs} ), See Notes 5 and 6 and Figure 3</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{rr} )</td>
<td>Reverse-recovery time</td>
<td>( I_F = 100 \text{ mA}, di/dt = 20 \text{ A/μs} ), See Notes 5 and 6 and Figure 3</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

NOTES: 5. Technique should limit \( T_J - T_C \) to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{θ JA} )</td>
<td>Thermal resistance, junction-to-ambient</td>
<td>DW package</td>
<td>All 8 outputs with equal power</td>
<td>90</td>
</tr>
<tr>
<td>( R_{θ JA} )</td>
<td>Thermal resistance, junction-to-ambient</td>
<td>N package</td>
<td>All 8 outputs with equal power</td>
<td>95</td>
</tr>
</tbody>
</table>

PARAMETER MEASUREMENT INFORMATION

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: \( t_r \leq 10 \text{ ns}, t_f \leq 10 \text{ ns}, t_w = 300 \text{ ns}, \) pulsed repetition rate (PRR) = 5 kHz, \( Z_O = 50 \text{ Ω} \).
B. \( C_L \) includes probe and jig capacitance.
PARAMETER MEASUREMENT INFORMATION

NOTES:  A. The word generator has the following characteristics: \( t_r \leq 10 \text{ ns}, t_f \leq 10 \text{ ns}, t_w = 300 \text{ ns}, \) pulsed repetition rate (PRR) = 5 kHz, \( Z_O = 50 \Omega \).
B. \( C_L \) includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES:  A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The \( V_{GG} \) amplitude and \( R_G \) are adjusted for \( di/dt = 20 \text{ A/µs} \). A \( V_{GG} \) double-pulse train is used to set \( I_F = 0.1 \text{ A} \), where \( t_1 = 10 \text{ µs}, t_2 = 7 \text{ µs}, \) and \( t_3 = 3 \text{ µs} \).

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode
### PARAMETER MEASUREMENT INFORMATION

#### SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

- **Word Generator (see Note A)**
- **VCC**
- **DOUT**
- **GND**
- **V(DD)DSX = 50 V**
- **VCC = 5 V**

#### NOTES:

A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.

B. Input pulse duration, $t_w$, is increased until peak current $I_{AS} = 0.5$ A.

Energy test level is defined as $E_{AS} = I_{AS} \times V(DD)DSX \times t_{av}/2 = 30$ mJ.

**Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

### TYPICAL CHARACTERISTICS

#### PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

- **$I_{AS}$ – Peak Avalanche Current – A**
- **$t_{av}$ – Time Duration of Avalanche – ms**

**Figure 5**

#### SUPPLY CURRENT vs FREQUENCY

- **$V_{CC} = 5$ V**
- **$T_C = -40$ °C to 125 °C**

**Figure 6**

---

**Notes:**

- **Note A:** The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.

- **Note B:** Input pulse duration, $t_w$, is increased until peak current $I_{AS} = 0.5$ A.

Energy test level is defined as $E_{AS} = I_{AS} \times V(DD)DSX \times t_{av}/2 = 30$ mJ.
TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE

\[ V_{CC} = 5 \text{ V} \]
See Note A

\[ T_C = 125\,^\circ\text{C} \]

\[ T_C = 25\,^\circ\text{C} \]

\[ T_C = -40\,^\circ\text{C} \]

\[ \Omega \]

Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

\[ V_{CC} \]

\[ \text{Logic Supply Voltage} - V \]

\[ I_D = 100 \text{ mA} \]
See Note A

\[ T_C = 125\,^\circ\text{C} \]

\[ T_C = 25\,^\circ\text{C} \]

\[ T_C = -40\,^\circ\text{C} \]

\[ \Omega \]

Figure 8

SWITCHING TIME

\[ T_J - T_C \]

\[ 10^\circ\text{C} \]

\[ \text{ns} \]

\[ T_J \]

\[ T_L \]

\[ T_{PLH} \]

\[ T_{PHL} \]

Figure 9

NOTE C: Technique should limit \( T_J - T_C \) to \( 10^\circ\text{C} \) maximum.
THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

\[ I_D = \text{Maximum Continuous Drain Current} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_C = 25^\circ \text{C} \]

\[ T_C = 100^\circ \text{C} \]

\[ T_C = 125^\circ \text{C} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_C = 25^\circ \text{C} \]

\[ t_w/t_{period} = 1 \text{ ms}/t_{period} \]

\[ d = 10\% \]

\[ d = 20\% \]

\[ d = 50\% \]

\[ d = 80\% \]

N – Number of Outputs Conducting Simultaneously

**Figure 10**

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

\[ I_D = \text{Maximum Peak Drain Current} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_C = 25^\circ \text{C} \]

\[ t_w/t_{period} = 1 \text{ ms}/t_{period} \]

\[ d = 10\% \]

\[ d = 20\% \]

\[ d = 50\% \]

\[ d = 80\% \]

N – Number of Outputs Conducting Simultaneously

**Figure 11**

Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REV</th>
<th>PAGE</th>
<th>SECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>5/18/05</td>
<td>A</td>
<td>5</td>
<td>Figure 1</td>
<td>Changed SRCLR timing diagram</td>
</tr>
<tr>
<td>7/1995</td>
<td>*</td>
<td></td>
<td></td>
<td>Original reversion</td>
</tr>
</tbody>
</table>

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPIC6B595DW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>TBD</td>
<td>CU NIPDAU</td>
<td>Level-1-220C-UNLIM</td>
</tr>
<tr>
<td>TPIC6B595DWG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>TPIC6B595DWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>TBD</td>
<td>CU NIPDAU</td>
<td>Level-1-220C-UNLIM</td>
</tr>
<tr>
<td>TPIC6B595N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>20</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information andDisclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**N (R-PDIP-T**)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

<table>
<thead>
<tr>
<th>PINS **</th>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
<td></td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
<td></td>
</tr>
<tr>
<td>MS-001 VARIATION</td>
<td>AA</td>
<td>BB</td>
<td>AC</td>
<td>AD</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS-013 variation AC.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
<th>URL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>Audio</td>
<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
</tr>
<tr>
<td>Data Converters</td>
<td>Automotive</td>
<td><a href="http://www.ti.com/automotive">www.ti.com/automotive</a></td>
</tr>
<tr>
<td>DSP</td>
<td>Broadband</td>
<td><a href="http://www.ti.com/broadband">www.ti.com/broadband</a></td>
</tr>
<tr>
<td>Interface</td>
<td>Digital Control</td>
<td><a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a></td>
</tr>
<tr>
<td>Logic</td>
<td>Military</td>
<td><a href="http://www.ti.com/military">www.ti.com/military</a></td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Optical Networking</td>
<td><a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a></td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Security</td>
<td><a href="http://www.ti.com/security">www.ti.com/security</a></td>
</tr>
<tr>
<td></td>
<td>Telephony</td>
<td><a href="http://www.ti.com/telephony">www.ti.com/telephony</a></td>
</tr>
<tr>
<td></td>
<td>Video &amp; Imaging</td>
<td><a href="http://www.ti.com/video">www.ti.com/video</a></td>
</tr>
<tr>
<td></td>
<td>Wireless</td>
<td><a href="http://www.ti.com/wireless">www.ti.com/wireless</a></td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated