WINSTAR Display
華凌光電股份有限公司

MODULE NO:
WATN001002BFW00000000
SPECIFICATION

CUSTOMER:

APPROVED BY	
PCB VERSION	
DATE	

FOR CUSTOMER USE ONLY

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

ISSUED DATE:

E-Paper Specification

Content:

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2009/03/20		First issue

Module Classification Information

WA	T	N	001002	B	F	W	0000000
①	②	③	④	⑤	⑥	⑦	⑧

① Brand：WINSTAR DISPLAY CORPORATION

② IC Type：T→Tab Type, C→COB Type

③ Display Type：N→ ICON Type

④ Model serials no.

⑤ Display Color　B→Black & White

⑥ Back Plan Type：　P→PCB
F→FPC

⑦ Module Type　W→Winstar
D→Custom

⑧ Special Code

General Decription:

The Winstar electronic paper technology an electrophoretic display module , the module like display film is thin, light weight, flexible and durable, the electrophoretic display feature:

◎ High whiteness
◎ High contrast ratio
◎ Sunlight readable
◎ 180° view angle
◎ Bi-stable(don't need power to retain an image)

1. General Specification:

Item	Dimension	Unit
Number of Segment	10 ICON x 2	—
Module dimension	73 x 46.7 x 0.5(MAX)	mm
View area	65.8 x 24.7	mm
EDP type	Black/White	
View direction	All direction	

2. Absolute Maximum Rating:

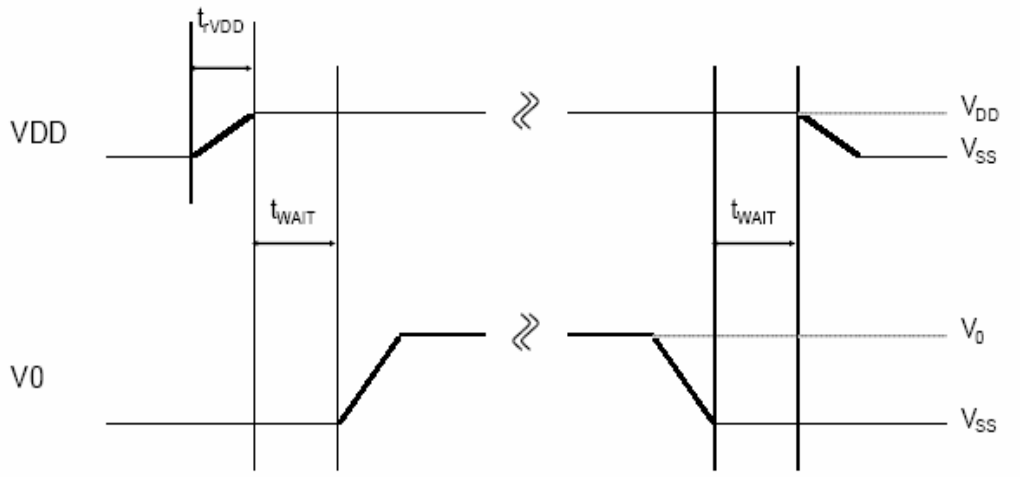
Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	0	—	+50	℃
Storage Temperature	T_{ST}	-35	—	+60	℃
Input Voltage	V_I	0	—	V_{DD}	V
Supply Voltage For Logic	V_{DD}	0	—	5.5	V
Supply Voltage For EPD	V0-V	0	—	40	V

3. Electrical Characteristics:

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	**2**	**5.0**	**5.5**	V
Supply Voltage For EPD	**V_0-V_{SS}**	—	**30**	**35**	**40**	**V**
Input High Volt.	**V_{IH}**	—	**2.0**	—	**V_{DD}**	**V**
Input Low Volt.	**V_{IL}**	—	**0**	—	**0.8**	**V**
Output High Volt.	**V_{OH}**	—	**2.4**	—	**V_{DD}**	**V**
Output Low Volt.	**V_{OL}**	—	**0**	—	**0.4**	**V**
Supply Current	**I_{DD}**	—	**0.2**	—	**0.84**	**mA**

3.1 Precautions with connecting or disconnecting the power:

This figure above is example for power supply sequence of power supply pin.Recommended power ON/OFF conditions:
trVDD (VDD rise time) < 20 ms
tWAIT (Waiting time between VDD and V0) > 20 ms



3.2 DC Characteristics: **(VSS= 0 V, VDD =+2.5 V, V0 = 40.0 V, TOPR=25 °C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Applicable pins
Input "High" voltage	VIH		0.8VDD		VDD	V	Pins 1
Input "Low" voltage	VIL		VSS		0.2VDD	V	
Output "High" voltage	VOH	IOH=- 0.4mA	VDD-0.4			V	EIO1, EIO2
Output "Low" voltage	VOL	IOL=+ 0.4mA			+ 0.4	V	
Input "High" current	IIH	VI= VDD			+ 10	μA	Pins 1
Input "Low" current	IIL	VI= VSS			- 10	μA	
Output resistance	RON1	Condition 1		4	8	kΩ	Y1-Y160
	RON2	Condition 1		500	800	Ω	Y0,Y161
Output OFF leakage current	IOFF				20	nA	Y1-Y160
Stand-by current	IDDS	Condition 2			10	μA	VDD
	I0S	Condition 2			10	μA	V0
Supply current (1) (De-selection)	IDD1	Condition 3			1.2	mA	VDD
Supply current (2) (Selection)	IDD2	Condition 4			7.2	mA	VDD
V0 Supply current	I0	Condition 5			1.0	mA	V0
		Condition 6			100	μA	

Pins 1: XCK, DI2-DI0, EIO1, EIO2, SHL, LATCH, SLEEPB, DLY1, DLY0, TEST
Condition 1: |ΔVON| = 0.5V, V0 = +40 V, V1 = +26 V, V2 = +13 V
Condition 2: VDD = 5V, V0 = 40V, VI = VSS
Condition 3: VDD = 5V, V0 = 40V, EIO(input) = VDD, fXCK = 12MHz, No output load
Condition 4: VDD = 5V, V0 = 40V, EIO(input) = VSS, fXCK = 12MHz, No output load
Condition 5: VDD = 5V, V0 = 40V, SLEEPB = VDD, fXCK = 12MHz, fLATCH = 25kHz, No output load
Condition 6: VDD = 5V, V0 = 40V, SLEEPB = VDD, fXCK = 500kHz, fLATCH = 1kHz, No output load

4. Optical Characteristics:

(1) Bi-Stability is the time which EPD can keep image contrast ratio larger than contrast ratio minimum specification.

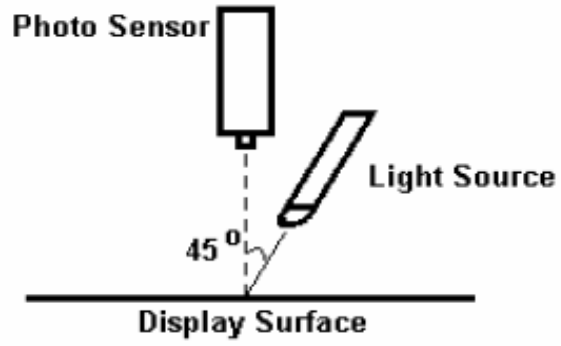
Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
White State Reflectance	RWhite	0~50℃	25	28		%	Note 4.3
View Angle	(V)θ	—	5	—	175	deg	----
	(H)φ	—	5	—	175	deg	----
Contrast Ratio	CR	0~9℃	3:1	5:1	—	—	Note 4.4
		10~19℃	4:1	6:1			Note 4.4
		20~50℃	7:1	8:1			Note 4.4
Response Time	Black to White	25℃	—	450	—	ms	7-5-7waveform
Bi-Stability	BiS	0℃	48			Hr	(1)
		25℃	72			Hr	(1)
		50℃	48			Hr	(1)

4.2 Test Methodology:

Performance of WINSTAR E-Paper module depends on many factors, such as driving waveform and temperature. All optical characteristics and tests are performed by PCB backplane without protection film or barrier film on top of EPD film except explicit indication. The tests are in controlled environments under the listed conditions.

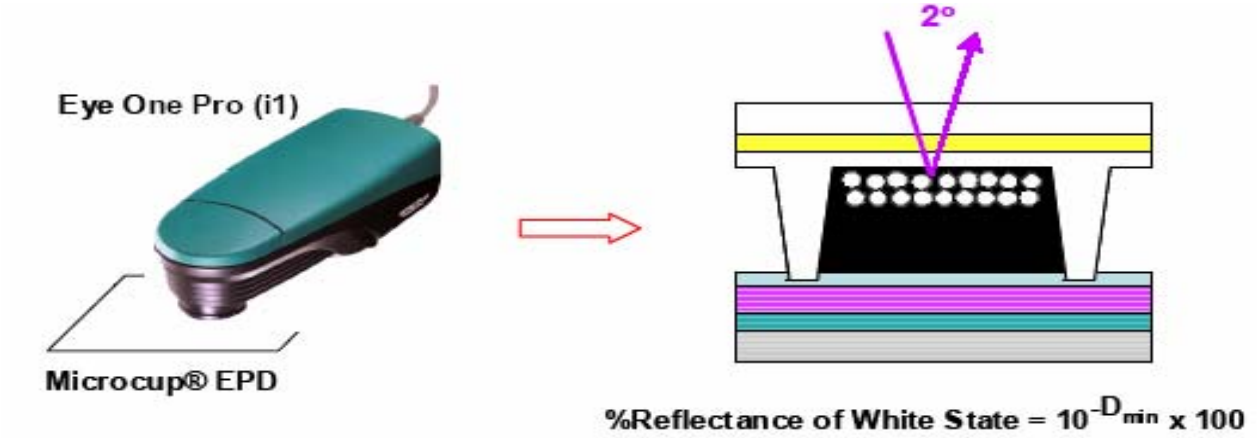
4.3 Optical Measurement System:

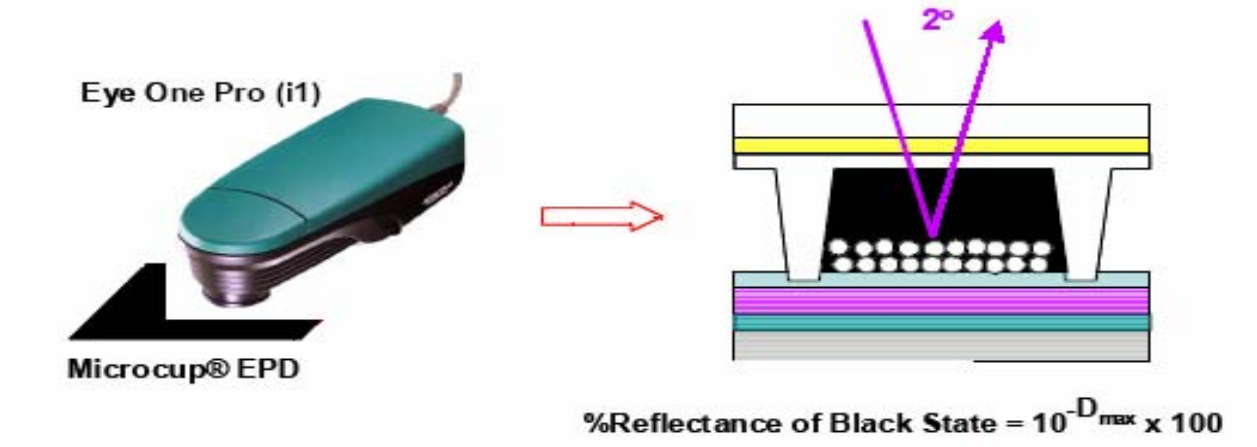
An optical measurement system (spectro-densitometer) is used to record the reflectance of WINSTAR E-paper module. In this specification, the measurement machine is Eye One Pro(i1) by GretagMacbeth. The measurement point is the center of Active Area if not specified individually. The measurement mechanism of i1 shows in the following figure.



4.4 Definition of Contrast Ratio:

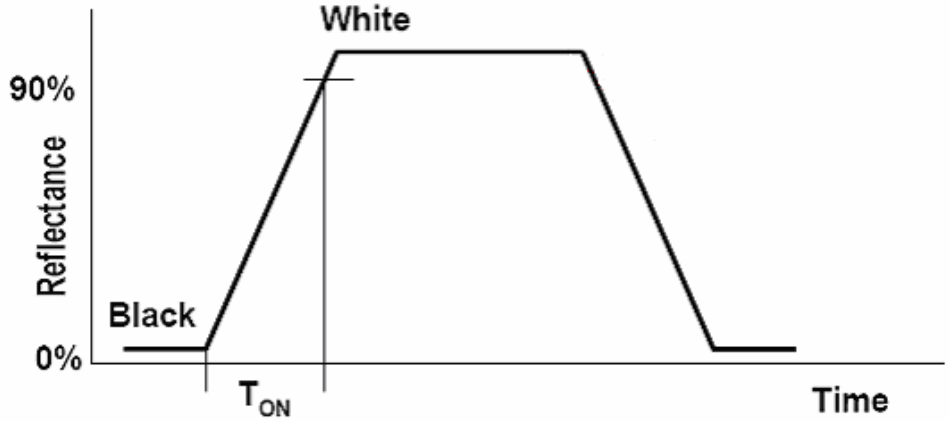
Contrast Ratio(CR)= %Reflectance of "white" state / %Reflectance of "black" state





4.5 Definition of response time:

The response time is measured by photo detector(photodiode) which measures the light intensity of active area center. The waveform follows section Page14.



TON is the time for a photo detector output waveform to go from 0% value to 90% of its maximum

5.Interface Description: Input1&Input2

Pin No.	Symbol	Description
1	V0	Base power supply pin for EPD drive voltage
2	V1	Base power supply pin for EPD drive voltage
3	V2	Base power supply pin for EPD drive voltage
4	VSSE	Base power supply pin for EPD drive voltage
5	VSS	Ground pin
6	EIO1	Input/output pin for chip selection
7	XCK	Clock input pin for taking display data
8	VDD	Logic system power supply pin
9	LATCH	Latch pulse input pin for display data
10	RESER VED	NC
11	SHL	Input pin for selecting the shift direction of display data
12	SLEEPB	Control input pin for dirver to enter power saving mode
13	DLY0	Input pin for selecting the driver output timing
14	DLY1	Input pin for selecting the driver output timing
15	RESER VED	NC
16	DI0	Input pin for display data
17	DI1	Input pin for display data
18	DI2	Input pin for display data
19	RESER VED	NC
20	EIO2	Input/output pin for chip selection
21	VSS	Ground pin
22	VSSE	Base power supply pin for EPD drive voltage
23	V2	Base power supply pin for EPD drive voltage
24	V1	Base power supply pin for EPD drive voltage
25	V0	Base power supply pin for EPD drive voltage
26	RESER VED	NC

5.1 Functional Operations

When the number of row/column is larger than 162, two or more DSM040 ICs are cascaded using EIO1 and EIO2. In this case, the EIO(output) of the first instance in the cascaded driver ICs is connected to the EIO(input) of the second one.

After all image data is stored in the Sampling Memory, the DSM040 is ready to drive the selected voltage to the display. After LATCH pulse falling edge, each output pin drives voltage according to the stored data.

Truth Table:

Hold Memory Data			SLEEPB	Driver Output Voltage level (Y0-Y161)
DI2	DI1	DI0		
0	X	X	H	High-Z
1	0	0	H	V0
1	0	1	H	V1
1	1	0	H	V2
1	1	1	H	VSSE
X	X	X	L	VSSE

X: Don't care, High-Z: High impedance

"Don't care" should be fixed to "1" or "0", avoiding floating.

Relationship between the Display Data and Driver Output pins

Here, L: VSS H: VDD:

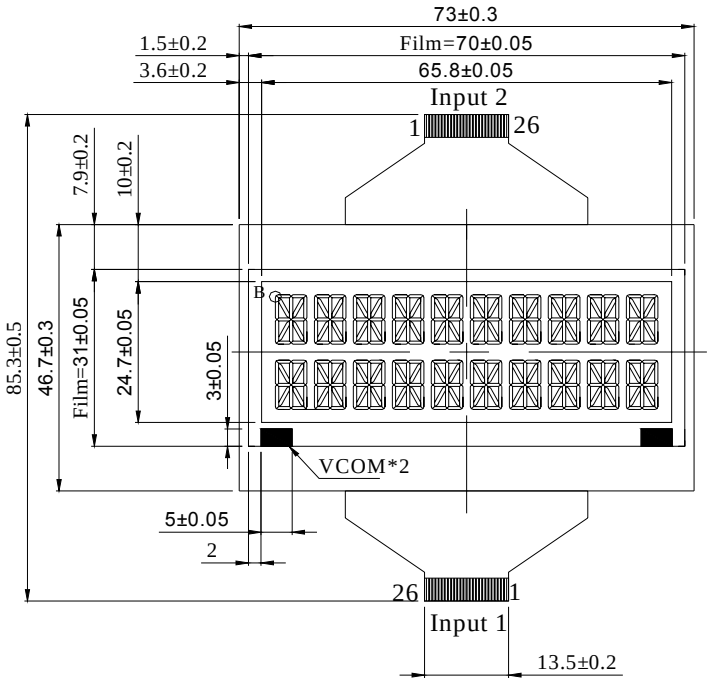
SHL	EIO1	EIO2	Figure of Clock						
			1clock	2clock	3clock	..	160clock	161clock	162clock
L	Output	Input	Y161	Y160	Y159	..	Y2	Y1	Y0
H	Input	Output	Y0	Y1	Y2	..	Y159	Y160	Y161

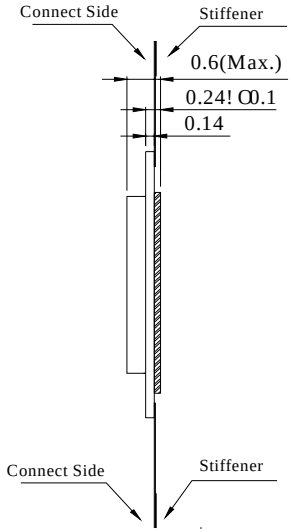
Status Table:

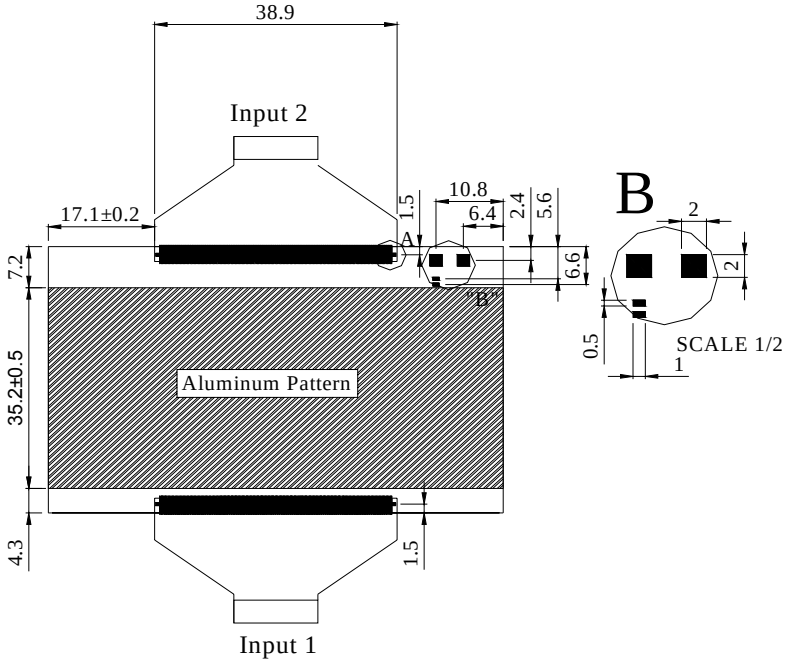
Here, L: VSS H: VDD

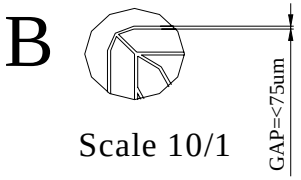
Mode	Power-on	Sleep
Condition	---	SLEEPB=L
Sampling Memory	Set to 111	Hold
Hold Memory	Set to 111	Hold
Y0 to Y161	VSSE	VSSE

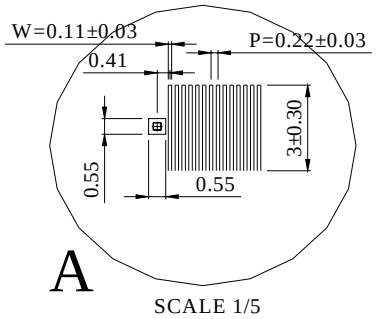
6. Contour Drawing & Block Diagram:

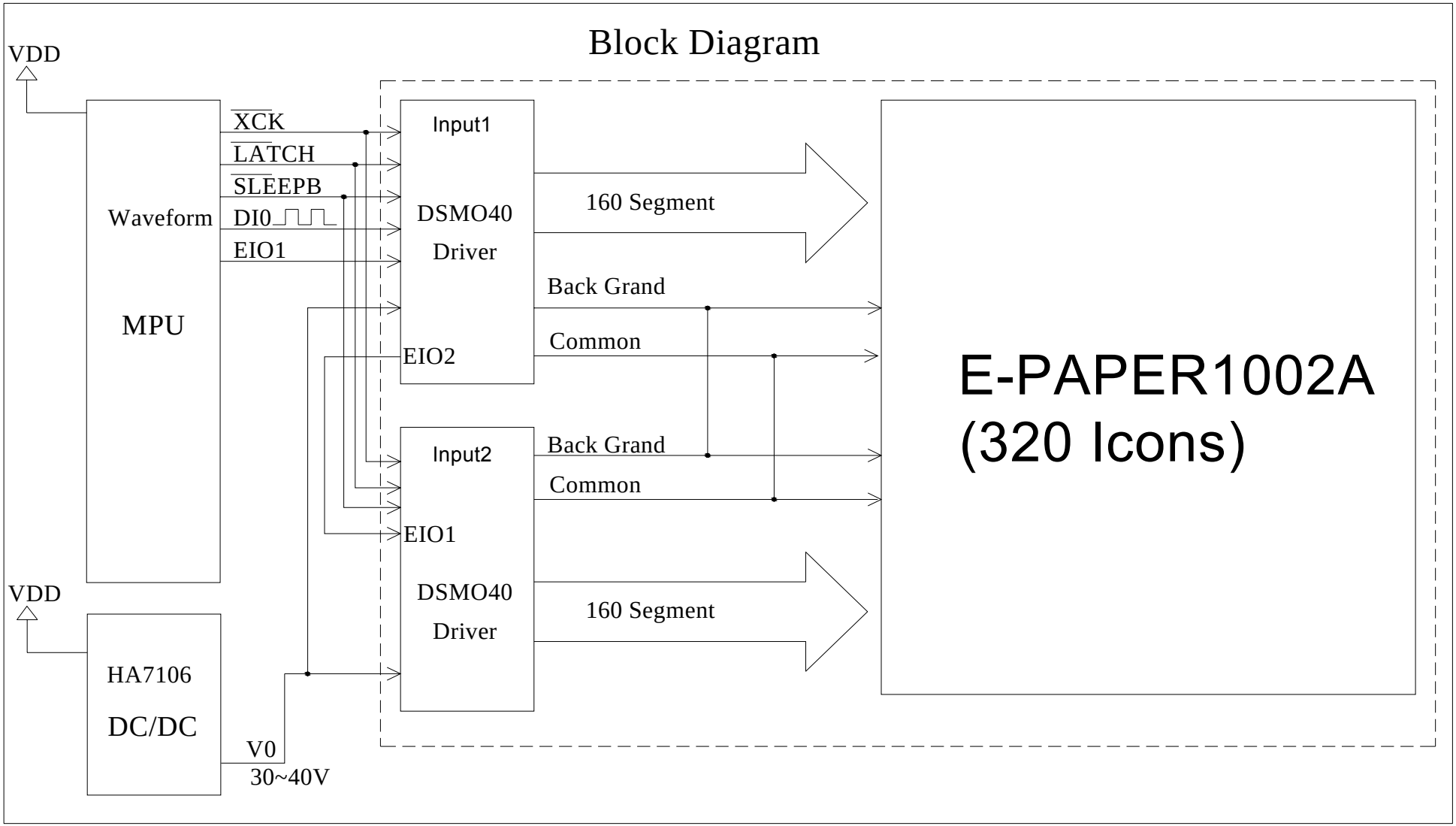




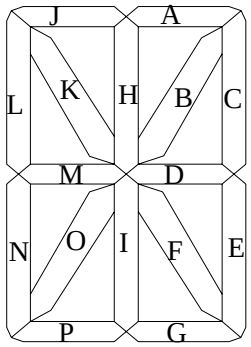






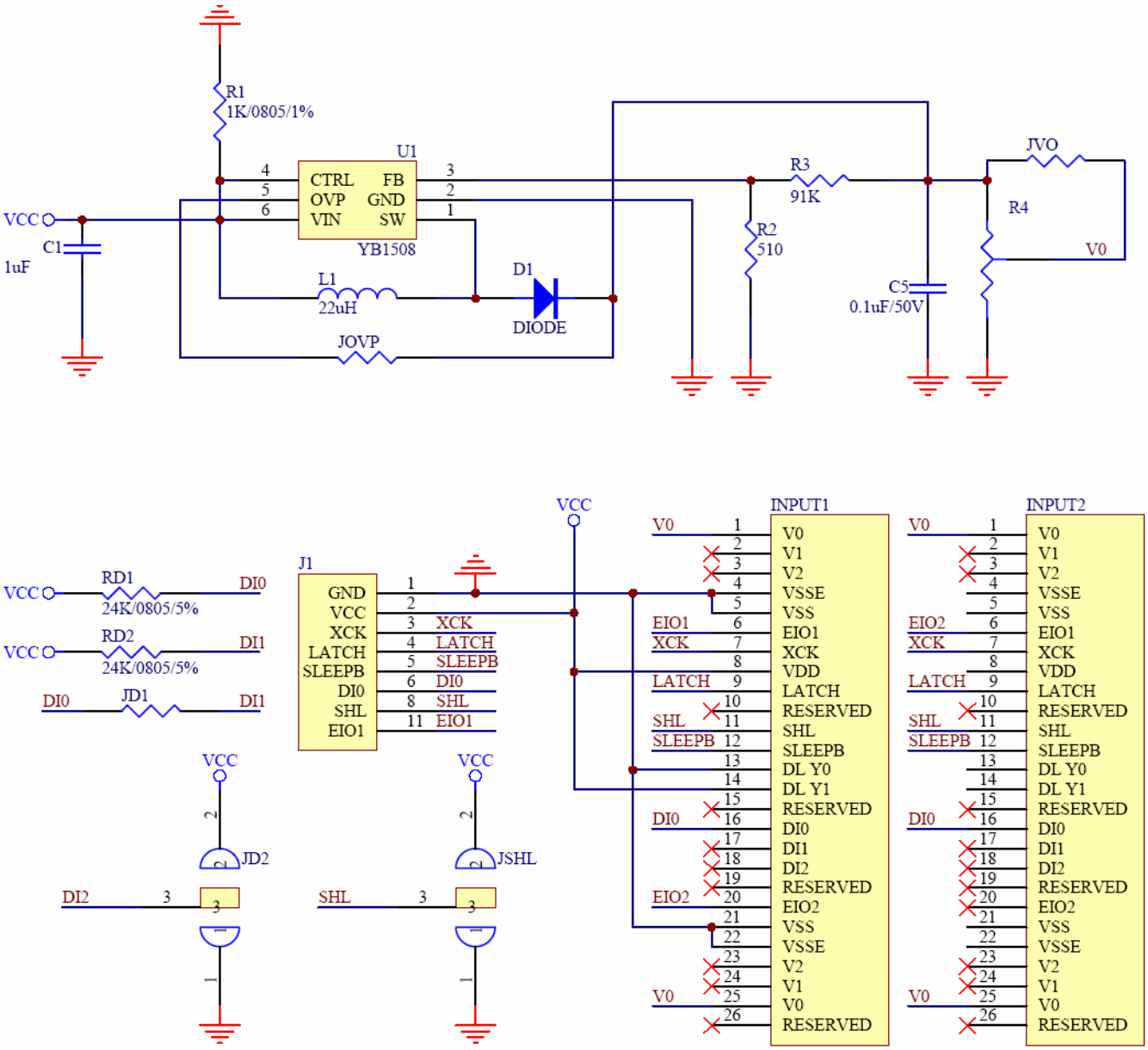

Block Diagram
VDD
Waveform
MPU
XCK
LATCH
SLEEPB
DI0
EIO1
Input1
DSMO40
Driver
160 Segment
Back Grand
Common
EIO2
Input2
Back Grand
Common
EIO1
DSMO40
Driver
160 Segment
E-PAPER1002A
(320 Icons)
VDD
HA7106
DC/DC
V0
30~40V

6.1COF Drive IC Interface Pin Assignment:



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
D1	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16
D2	Y17	Y18	Y19	Y20	Y21	Y22	Y23	Y24	Y25	Y26	Y27	Y28	Y29	Y30	Y31	Y32
D3	Y33	Y34	Y35	Y36	Y37	Y38	Y39	Y40	Y41	Y42	Y43	Y44	Y45	Y46	Y47	Y48
D4	Y49	Y50	Y51	Y52	Y53	Y54	Y55	Y56	Y57	Y58	Y59	Y60	Y61	Y62	Y63	Y64
D5	Y65	Y66	Y67	Y68	Y69	Y70	Y71	Y72	Y73	Y74	Y75	Y76	Y77	Y78	Y79	Y80
D6	Y81	Y82	Y83	Y84	Y85	Y86	Y87	Y88	Y89	Y90	Y91	Y92	Y93	Y94	Y95	Y96
D7	Y97	Y98	Y99	Y100	Y101	Y102	Y103	Y104	Y105	Y106	Y107	Y108	Y109	Y110	Y111	Y112
D8	Y113	Y114	Y115	Y116	Y117	Y118	Y119	Y120	Y121	Y122	Y123	Y124	Y125	Y126	Y127	Y128
D9	Y129	Y130	Y131	Y132	Y133	Y134	Y135	Y136	Y137	Y138	Y139	Y140	Y141	Y142	Y143	Y144
D10	Y145	Y146	Y147	Y148	Y149	Y150	Y151	Y152	Y153	Y154	Y155	Y156	Y157	Y158	Y159	Y160
COM	Y161															
B.G.	Y1															

6.2 Reference Circuit:



7. Display Driving Waveform:

Droving Waveform will depend on applications and requirements. The display module driving waveform and relative lookup table(LUT) are specific for each customer. All measurements and qualifications are using the following waveforms.

7.1 Temperature Range: 10ºC – 50ºC:

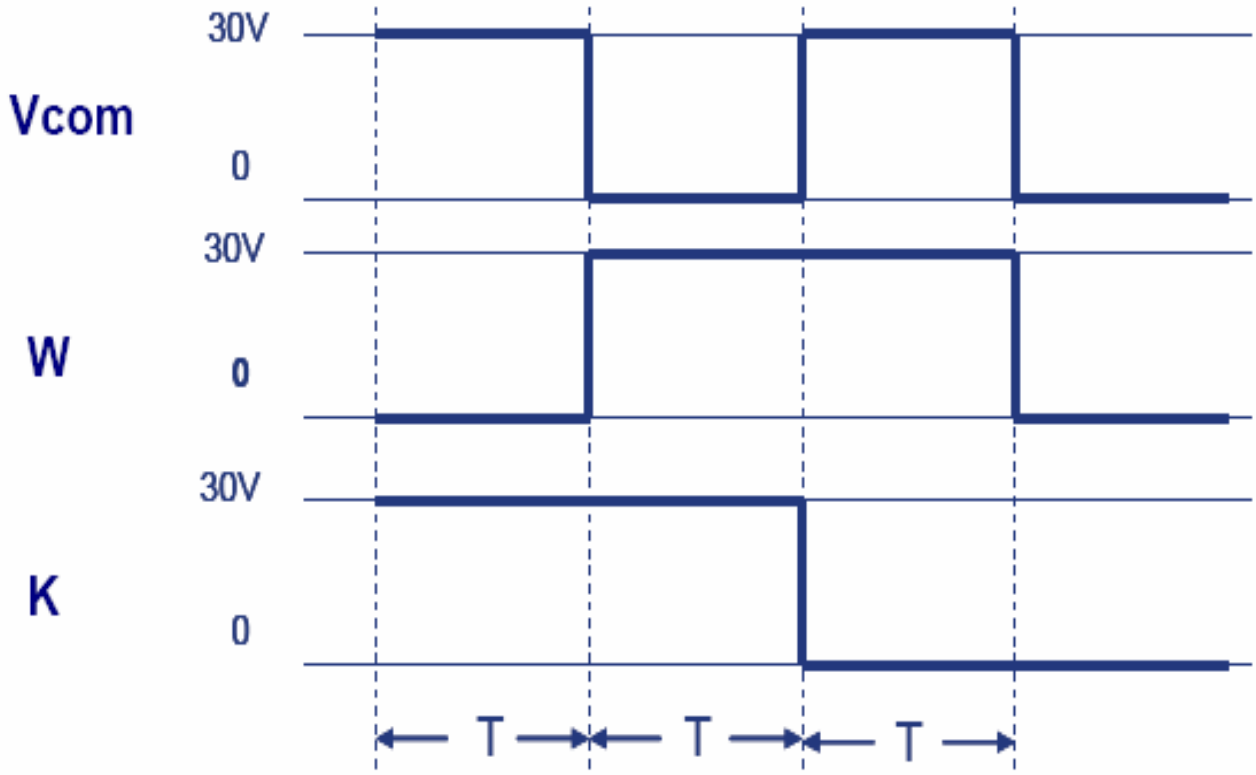


Table 3.1 Waveform duration for temperature range between 10°C – 50°C

Temerature Range (°C)	T (s)	Total Driving Time (s)
40 - 50	0.4	1.2
30 - 39	0.6	1.8
20 - 29	1	3
15 - 19	1.5	4.5
10 - 14	2	6

7.2 Temperature Range: 0ºC – 9ºC:

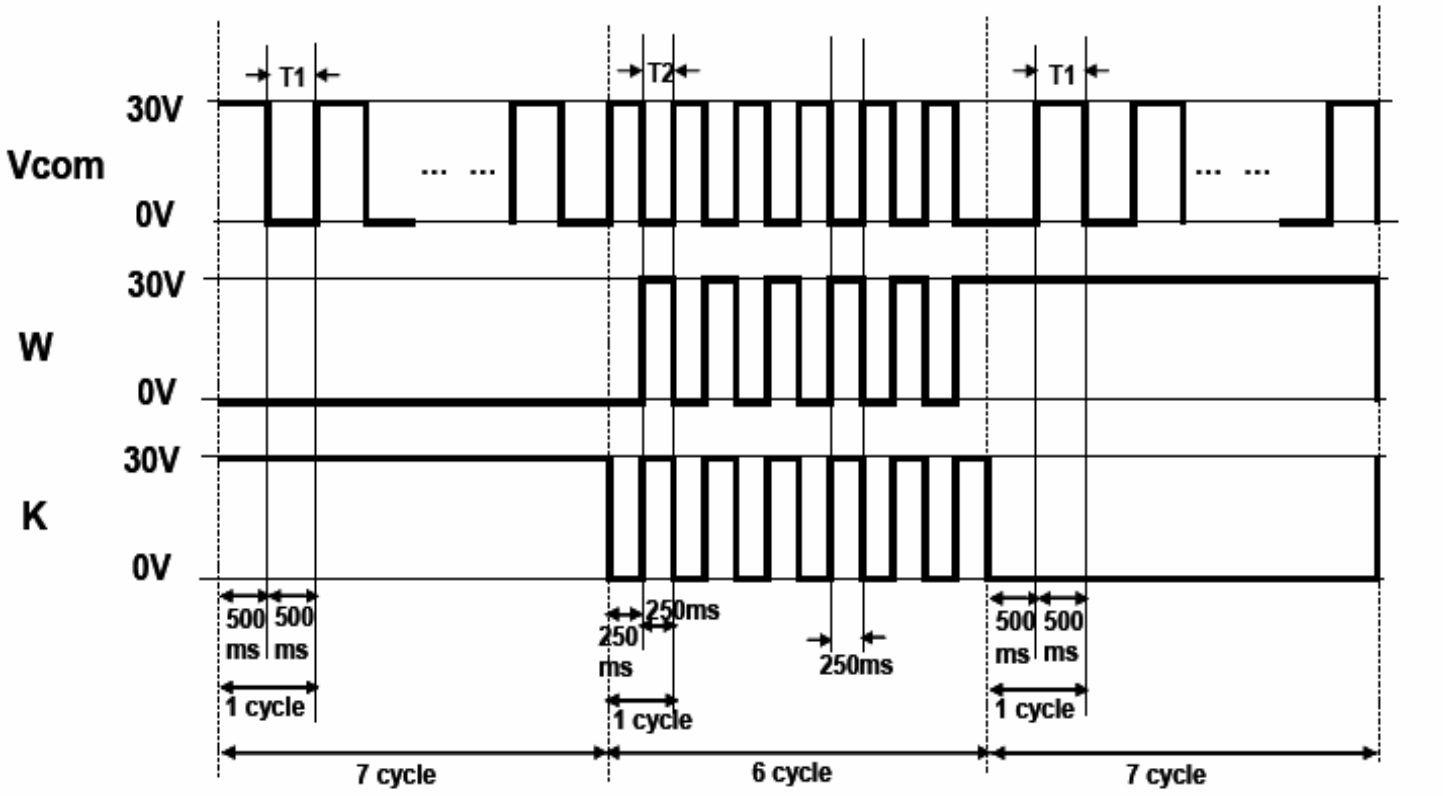
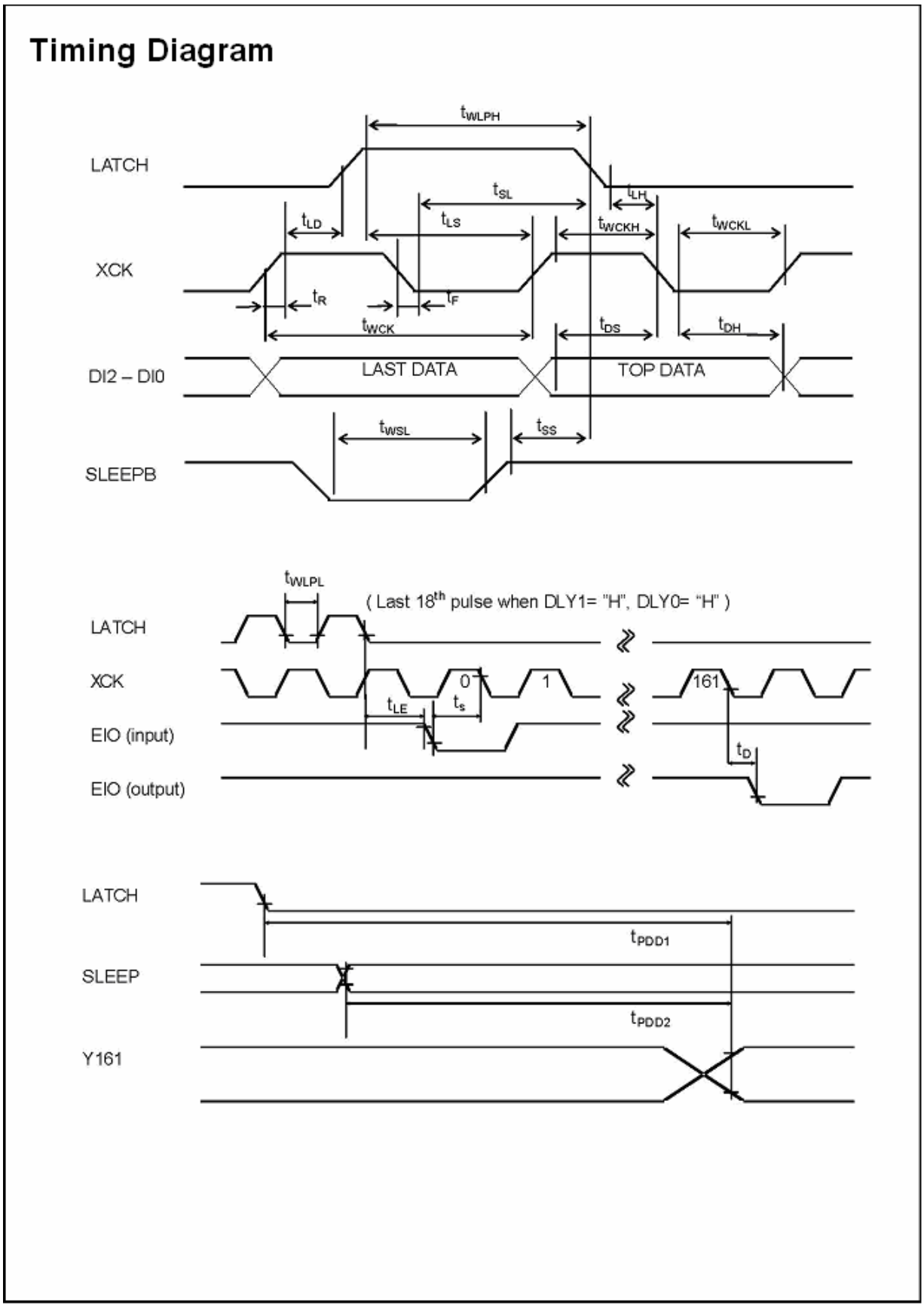


Table 3.2 Waveform duration for temperature range between 0°C – 9°C

Temperature Range	Waveform Name	T1	T2	Total Driving Time
0 - 9ºC	7-6-7	500ms	250ms	17s

8. Timing Diagram:

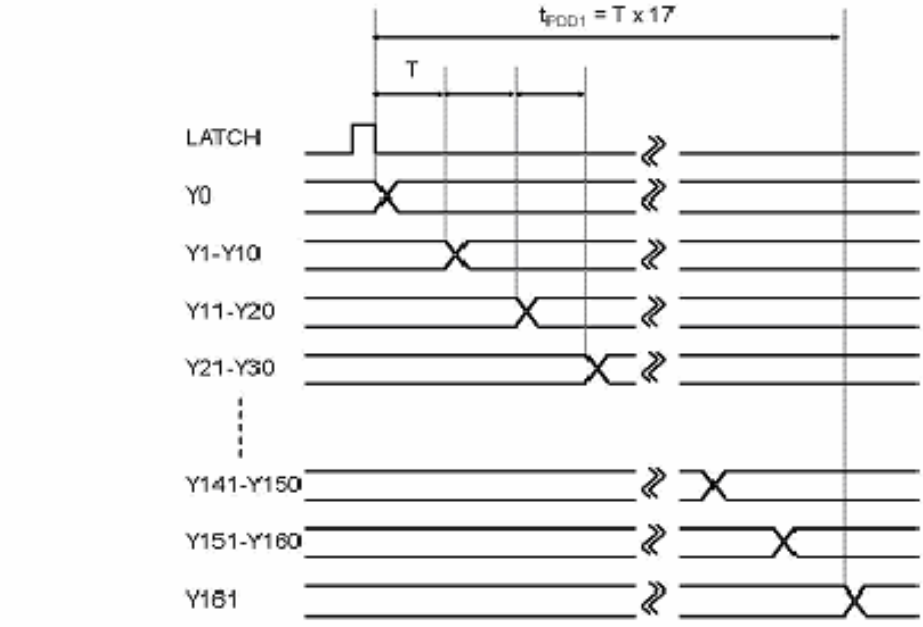


8-1. Timing AC Characteristics(VSS= 0 V, VDD = 5.0 V, V0 = 40.0 V, TOPR=25 °C)

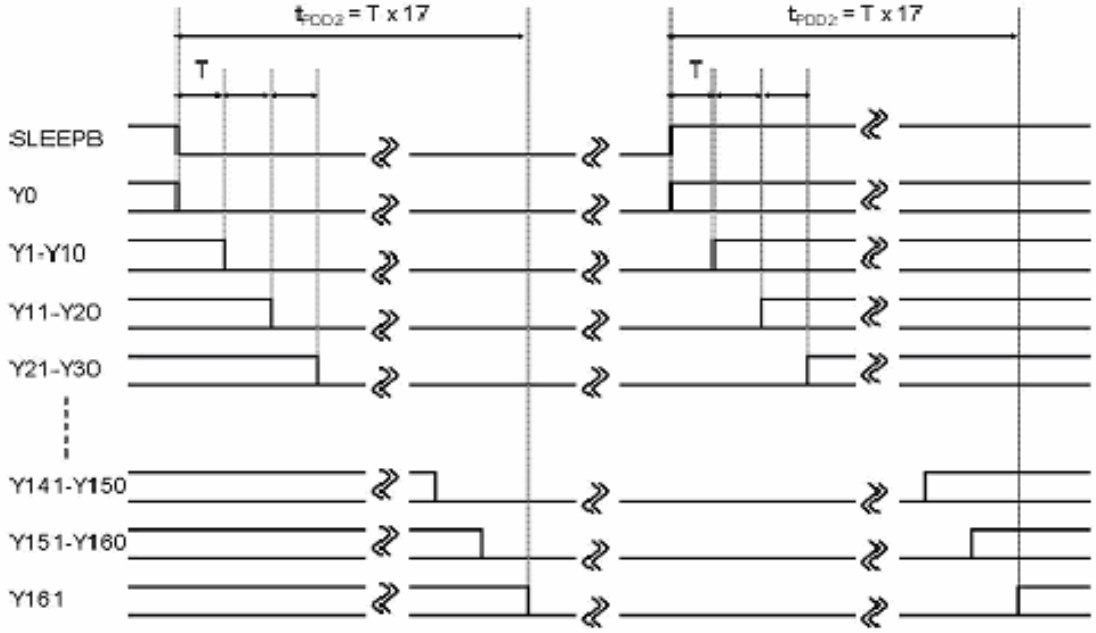
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Applicable Pins	NOTE
Shift clock period	tWCK	tR, tF ≤ 10 ns	80			ns	XCK	
Shift clock “H” pulse width	tWCKH		20			ns		
Shift clock “L” pulse width	tWCKL		20			ns		
Data setup time	tDS		20			ns	XCK, DI2-0	
Data hold time	tDH		30			ns		
Latch pulse “H” pulse width	tWLPH	DLY1= VDD, DLY0= VDD	20			ns	LATCH	
		DLY1= VDD, DLY0= VSS	2.5			µs		
Latch pulse “L” pulse width	tWLPL	DLY1= VDD, DLY0= VDD	20			ns		
Latch pulse fall to EIO input fall time	tLE	DLY1= VDD, DLY0=VSS	23			µs	LATCH EIO1,EIO2	
		DLY1= VDD, DLY0=VDD	100			ns		
Shift clock rise to Latch pulse rise time	tLD		0			ns	XCK, LATCH	
Shift clock fall to Latch pulse fall time	tSL		50			ns		
Latch pulse rise to Shift clock rise time	tLS		40			ns		
Latch pulse fall to Shift clock fall time	tLH		25			ns		
Input signal rise time	tR				50	ns	All input	Note 1
Input signal fall time	tF				50	ns	pins	Note 1
SLEEPB removal time	tSS	DLY1= VDD	23			µs	SLEEPB, LATCH	
SLEEPB “L” pulse width	tWSL		2.5			µs	SLEEPB	
EIO input setup time	tS		25			ns	XCK, EIO1, EIO2	
EIO output delay time	tD	CL=15pF			50	ns	XCK, EIO1, EIO2	
Y161 output delay time (1)	tPDD1	CL=15pF, DLY1=VDD, DLY0=VSS	2.4		50	µs	LATCH, Y161	
Y161 output delay time (2)	tPDD2	CL=15pF, DLY1=VDD,	2.4		50	µs	SLEEPB, Y161	

8-2. FPD Drive Output Timing

(1) DLY1 = “H”, DLY0 = ”L” The driver outputs levels are changed at intervals by internal delay circuits.



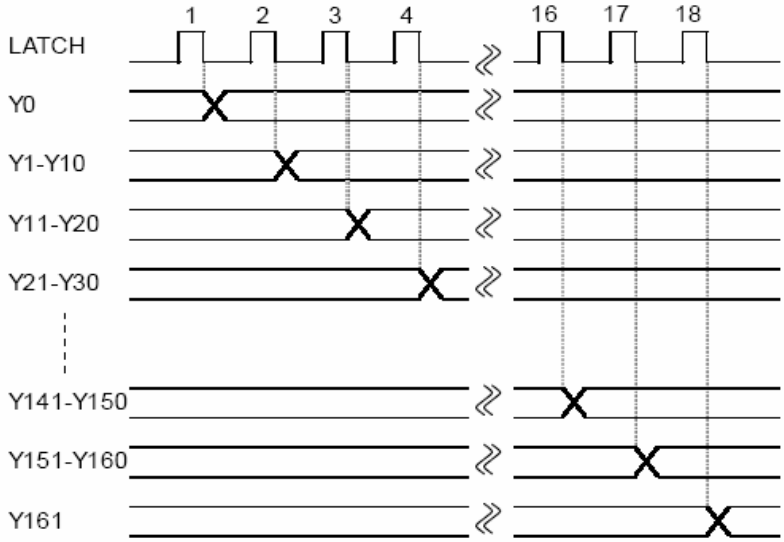
T : Interval time



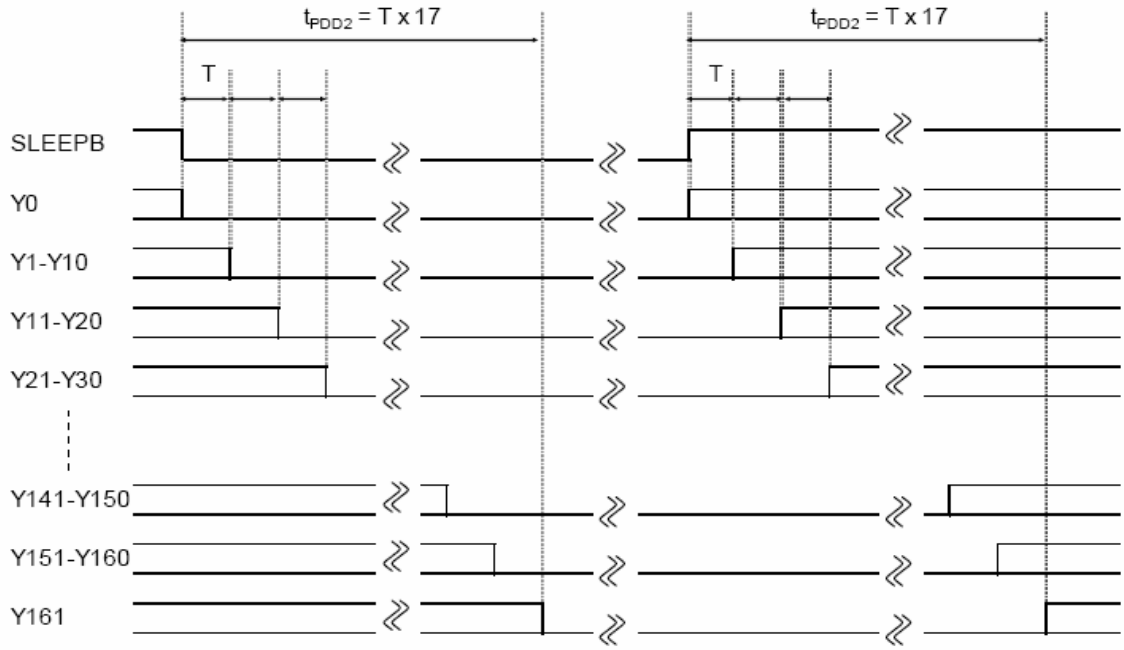
T : Interval time

play

(2) DLY1 = “H”, DLY0 = ”H” The driver outputs levels are changed at intervals by LATCH pulses.



When using sleep mode, the driver outputs levels are changed at intervals by internal delay circuits.



T : Interval time

9. Product Picture:

9-1.White Background & Black Icon:

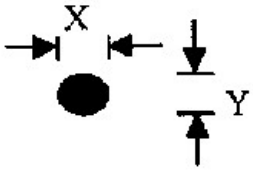
9-2. Black Background & White Icon:

10. Reliability Specifications:

	Test item	Test condition	Remark
1	High-Temperature Operation	Ta=+50°C,RH=30% For 240 hrs	Note 2
2	Low-Temperature Operation	Ta=0°C For 240 hrs	Note 2
3	High-Temperature Storage	Ta=+60°C For 240 hrs	Note 2
4	Low-Temperature Storage	Ta=-35°C For 240 hrs	Note 2
5	Bi-Stability	High Temp, 50°C, 48 hrs	Note 2
		Ambient , 25°C, 168 hrs	
		Low Temp, 0°C, 48 hrs	

Note 1 : Sample will be left in 25°C environment for 4 hours after finish the environmental test and take measurement after 7-5-7 waveform re-driving.
Note 2 : The judgment of above tests should satisfy electrical and optical requirement.
Note 3 : Anti-moisture layer and edge sealing are needed for all tests.

11. Inspection specification:

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing character , dot or icon.
1.2 Display malfunction.
1.3 No function or no display.
1.4 Current consumption exceeds product specifications.
1.5 Mixed product types.
1.6 Don’t operation or store EPD panels outside of specified range.</td><td>0.65</td></tr>
<tr><td>05</td><td>EPD Spots, Bubbles contamination (non-display)</td><td>Round type : As following drawing
Φ=(x + y) / 2
 

<table><tr><th>SIZE</th><th>Acceptable Q TY</th></tr><tr><td>Φ ≦0.15</td><td>Accept no dense</td></tr><tr><td>0.15＜Φ ≦0.3</td><td>5</td></tr><tr><td>0.3＜Φ ≦0.5</td><td>1</td></tr><tr><td>0.5＜Φ</td><td>0</td></tr></table></td><td>2.5</td></tr>
<tr><td>03</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>04</td><td>General appearance</td><td>4.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.
4.2 No cracks on interface pin (OLB) of TCP.
4.3 No contamination, solder residue or solder balls on product.
4.4 The IC on the TCP may not be damaged, circuits.
4.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever.
4.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.
4.7 Product packaging must the same as specified on packaging specification sheet.
4.8 Product dimension and structure must conform to product specification sheet.</td><td>2.5
0.65
2.5
2.5
2.5
2.5
0.65
0.65</td></tr>
</table>

12. Handling Precautions:

12.1 Wear anti static wrist strip when removing EPD module from antistatic bag.

12.2 When cleaning the display surface, use soft cloth with solvent recommended below and wipe lightly.

Ethyl alcohol
Isopropyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the EPD surface.

Do not use the following solvents:

Ketone
Aromatics

12.3 Don't ON/OFF the power during operation. Direct current causes electro-chemical reaction with remarkable degradation of the display quality.

12.4 Avoid strong shock and drop from a height.

12.5 Do not operate or store EPD panels outside of specified range.

13. Storage Condition:

13.1 Transportation:

Packaging: vacuum sealed aluminum bag with desiccant pack
Temperature range: -20oC < T < +60oC
Storage time: 10 days

13.2 Long Term Storage:

Packaging: vacuum sealed aluminum bag with desiccant pack
Temperature range: 20oC < T < 30oC
Storage time: 5 months after receipt of shipment

13.3 After Package is Open:

Packaging: no packaging, store in dry box
Humidity < 30%RH
Temperature range: 20oC < T < 25oC
Storage time: 1 month after receipt of shipment

13.4 Outside Dry Box during Assembly:

Packaging: none
Temperature range: 20oC < T < 30oC
Time <24 hours, if >24 hours, send back to dry box