2.1 The following documents of the issue in effect on the release date of this drawing (unless an exact issue is shown) form a part of this drawing to the extent specified herein. In an event of a conflict between this control drawing, the procurement document, and applicable documents, the order of precedence shall be the procurement document, this control drawing and the applicable document(s). For reference only unless specified elsewhere in this drawing.

INDUSTRY

ANSI/ASQC Z1.4 - 1993	Sampling Procedures and Tables for Inspection by Attributes
ANSI/ISO/ASQC Q9001-1994	Quality Systems - Model for Quality Assurance in Design/Development, Production, Installation and Servicing

OTHER

Renesas HD66790	Datasheet for Driver/Controller IC (main)
Renesas HD66782	Datasheet for Driver/Controller IC (sub)

3.1.1 Main Glass Display Specifications.

1. Transflective TFT Display; a-SI active matrix
2. Module size: 40.25 mm wide x 56.50 mm long (including frame)
3. Pixel Format: 240 x 3 x 320 (240 RGB Stripes x 320 rows), QVGA
4. Pixel Size: TBD mm wide (3 x TBD) x TBD mm long
5. Pixel Pitch: 0.141 mm wide x 0.141 mm long
6. Dots Per Inch: 180
7. Display Color: 262K colors, 18-Bit Parallel Data Input
8. Viewing Angle: 6 O'clock
9. Driver/Controller IC shall be Renesas HD66790.
10. The booster circuit of the gate driver IC shall be utilized to provide proper drive voltages.
11. Glass panel dimensions: 38.44mm wide x 54.72 mm long
12. Active Area Dimensions: 33.84mm wide x 45.12 mm long
13. The main glass panel assembly shall also include protective films on both sides of the glass.

3.1.2 Sub Glass Display Specifications.

1. Transmissive TFT Display; a-SI active matrix
2. Module size: 26.11 mm wide x 25.60 mm long (including frame)
3. Pixel Format: 128 x 3 x 96 (128 RGB Columns x 96 rows) QVGA
4. Pixel Size: TBD mm wide (3 x TBD) x TBD mm long
5. Pixel Pitch: 0.168 mm wide x 0.168 mm long
6. Dots Per Inch: 151
7. Display Color: 262K colors, 18-Bit Parallel Data Input
8. Viewing Angle: 6 O'clock
9. Driver/Controller IC shall be Renesas HD66782.
10. The booster circuit of the gate driver IC shall be utilized to provide proper drive voltages.
11. Glass panel dimensions: 26.11mm wide x 25.60 mm long
12. Active Area Dimensions: 21.504mm wide x 16.128 mm long
13. The main glass panel assembly shall also include protective films on both sides of the glass.

3.1.3 LED Backlighting Specifications.

1. Number of LEDs: 6
2. Color of LEDs: White
3. The LEDs will be side fire type (right angle).
4. The LEDs will be located on the Backlight Unit.
5. The LEDs are connected in parallel and require a separate current limiting circuit (part of phone circuit design).
6. The backlight unit shall also include a poron pad, double-sided adhesive gaskets, and protective films on both sides of the backlight unit.

Table 1. Electrical Specifications - Operating Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage (logic)	VCC	-	2.50	2.8	3.60	V
Power supply voltage (analog)	Vci	-	2.50	2.8	3.60	V
Power supply voltage (I/O)	IOVcc		1.65	2.8	3.6	V
Input voltage (logic)	Vi	'H' level	0.8 IOVcc	-	IOVcc	V
		'L' level	0	-	0.2 IOVcc	
Output voltage (logic)	Vo	'H' level Ioh=-0.1mA	0.7 IOVcc	-	-	V
		'L' level Iol=-0.1mA	-	-	0.15 IOVcc	
Power Consumption	B/L	6-LEDs	-	300	-	mW
	Panel	-	-	-	45	mW
LED forward voltage	VLED	-	-	3.5	-	V
LED Current	IL (per LED)			15	20	mA
Response Time	Tr + Tf	-	-	40	-	ms

1. Flex cable dimensions: See Figure 5 and 6.

Table 3. Main Flex Cable Pin-Out

No.	Name	Description	Remark
1	DUMMY1	Dummy	
2	2.8DV	LCD POWER	2.8V(typ)
3	2.8DV	LCD POWER	2.8V(typ)
4	B5 -> MSB	LCD DATA	
5	B4	LCD DATA	
6	B3	LCD DATA	
7	B2	LCD DATA	
8	B1	LCD DATA	
9	B0 -> LSB	LCD DATA	
10	G5 -> MSB	LCD DATA	
11	G4	LCD DATA	
12	G3	LCD DATA	
13	G2	LCD DATA	
14	G1	LCD DATA	
15	G0 -> LSB	LCD DATA	
16	R5 -> MSB	LCD DATA	
17	R4	LCD DATA	
18	R3	LCD DATA	
19	R2	LCD DATA	
20	R1	LCD DATA	
21	R0 -> LSB	LCD DATA	
22	GND	Ground	
23	MLCD_CS	SPI Main Chip Select	
24	D_SDA	SPI Serial data Input	
25	D_SCL	SPI Serial data Clock	
26	DOTCLK	Dot clock	
27	MLCD_RESET	Main LCD Reset	
28	HSYNC	Hsync	
29	VSYNC	Vsync	
30	DE	Data Enable	
31	GND	Ground	
32	GND	Ground	
33	DUMMY2	Dummy	

Table 4. Sub Flex Cable Pin-Out

No.	Name	Description	Remark
1	DUMMY1	Dummy	
2	DUMMY2	LCD POWER	
3	2.8DV	LCD POWER	2.8V(typ)
4	B5 -> MSB	LCD DATA	
5	B4	LCD DATA	
6	B3	LCD DATA	
7	B2	LCD DATA	
8	B1	LCD DATA	
9	B0 -> LSB	LCD DATA	
10	G5 -> MSB	LCD DATA	
11	G4	LCD DATA	
12	G3	LCD DATA	
13	G2	LCD DATA	
14	G1	LCD DATA	
15	G0 -> LSB	LCD DATA	
16	R5 -> MSB	LCD DATA	
17	R4	LCD DATA	
18	R3	LCD DATA	
19	R2	LCD DATA	
20	R1	LCD DATA	
21	R0 -> LSB	LCD DATA	
22	DUMMY3	Ground	
23	SLCD_CS	SPI Main Chip Select	
24	D_SDA	SPI Serial data Input	
25	D_SCL	SPI Serial data Clock	
26	DOTCLK	Dot clock	
27	SLCD_RESET	Main LCD Reset	
28	HSYNC	Hsync	
29	VSYNC	Vsync	
30	DE	Data Enable	
31	GND	Ground	
32	GND	Ground	
33	DUMMY4	Dummy	

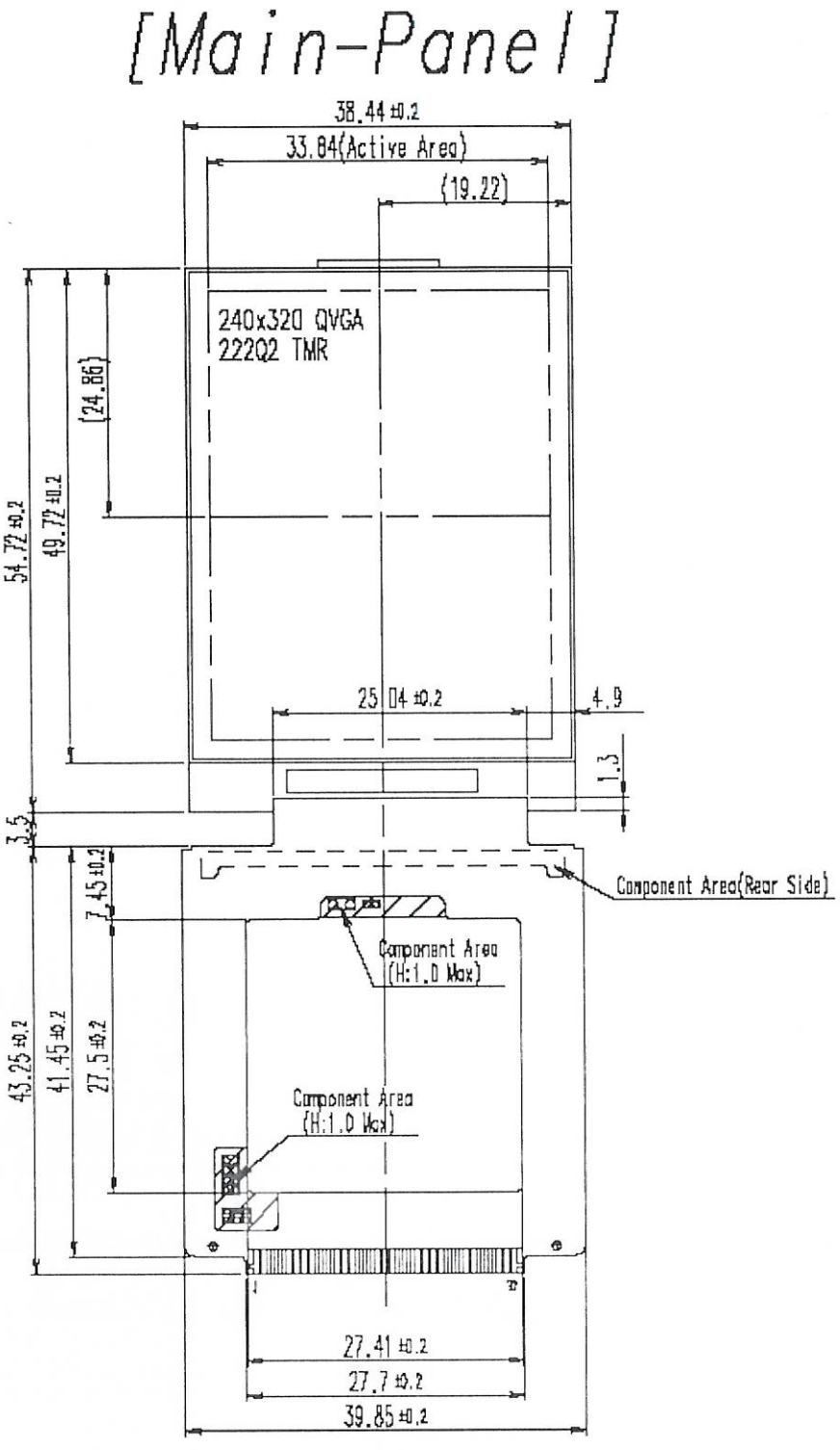

Figure 6. Main Panel Outline Drawing

[Sub-Panel]

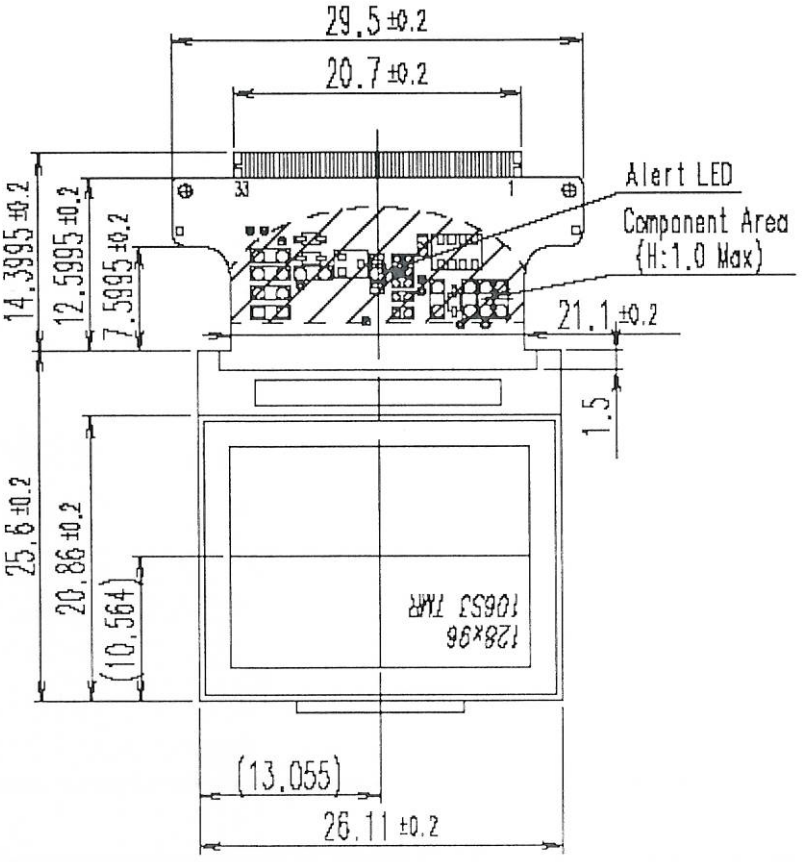

Figure 7. Sub Panel Outline Drawing

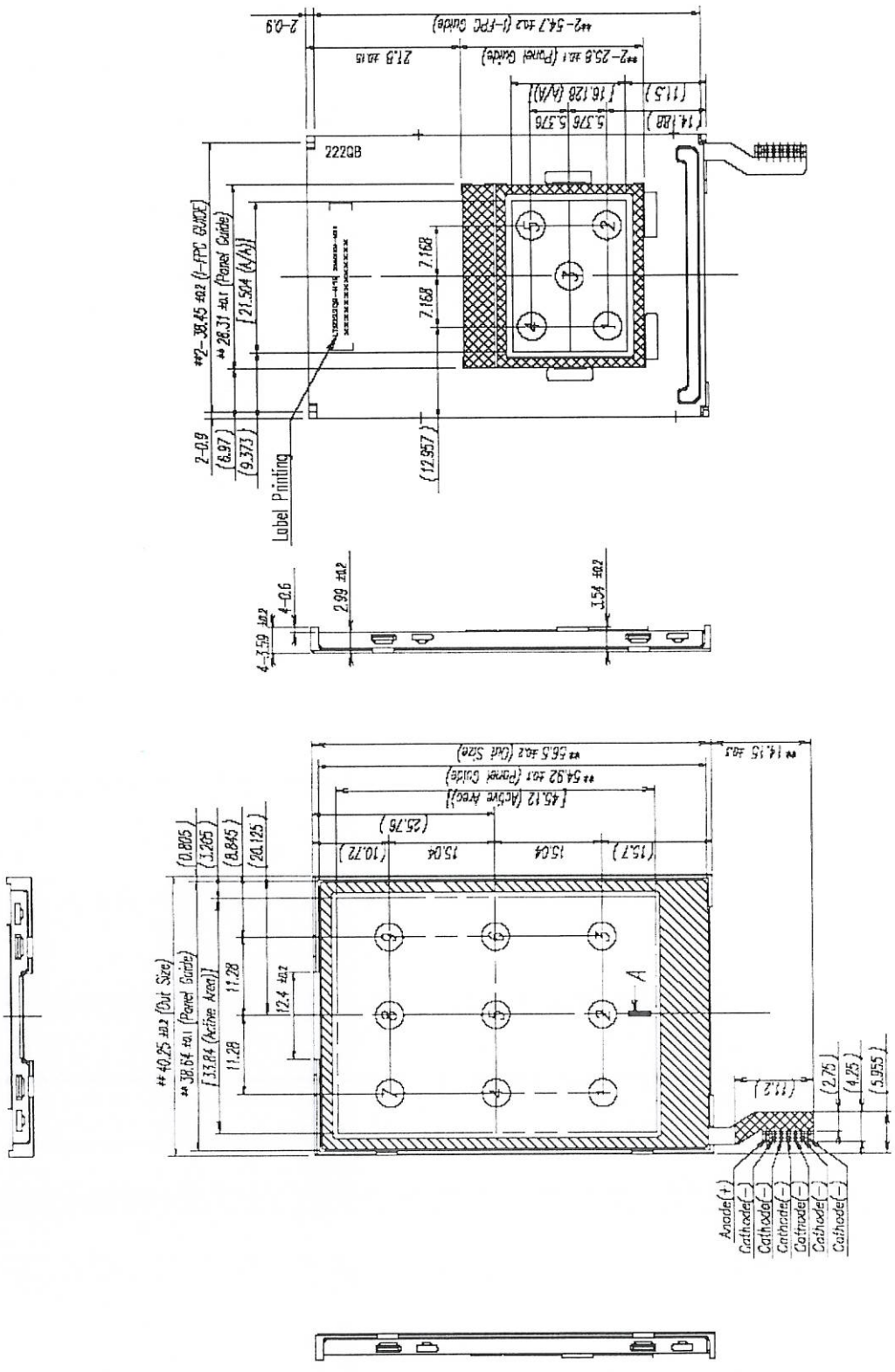

Figure 8. Backlight Unit (BLU) Outline Drawing